Description

The NE1185 is a controller designed specifically for the resonant half-bridge topology. It provides two drive-signal channels that output complementary signals at a 50% duty cycle. An internal fixed dead-time of 320ns between the two complementary gate signals guarantees zero-voltage switching during the transient and enables high-frequency operation.

The integrated bootstrap diode simplifies the external driving circuit for the high-side switch. It can withstand up to 600V with immunity against high dV/dt noise. Modulating the switching frequency regulates the topology output voltage. A programmable oscillator can set both the maximum and minimum switching frequencies.

The IC starts up at the programmed maximum switching frequency and gradually slows until the control loop takes over to prevent excessive inrush current.

The IC can be forced to enter a controlled burst-mode operation at light-load to minimize the power consumption and tighten output regulation.

IC's functions include a not-latched active-low disable input with current hysteresis useful for power sequencing or for brownout protection, a current sense input for OCP with frequency shift and delayed shutdown with automatic restart. A higher level OCP latches off the IC if the first-level protection is not sufficient to control the primary current. Their combination offers complete protection against overload and short circuits.

The IC provide 1A/2A source/sink capability for both high-side and low-side gate drivers.

The NE1185 is available in a SOP-16 package.

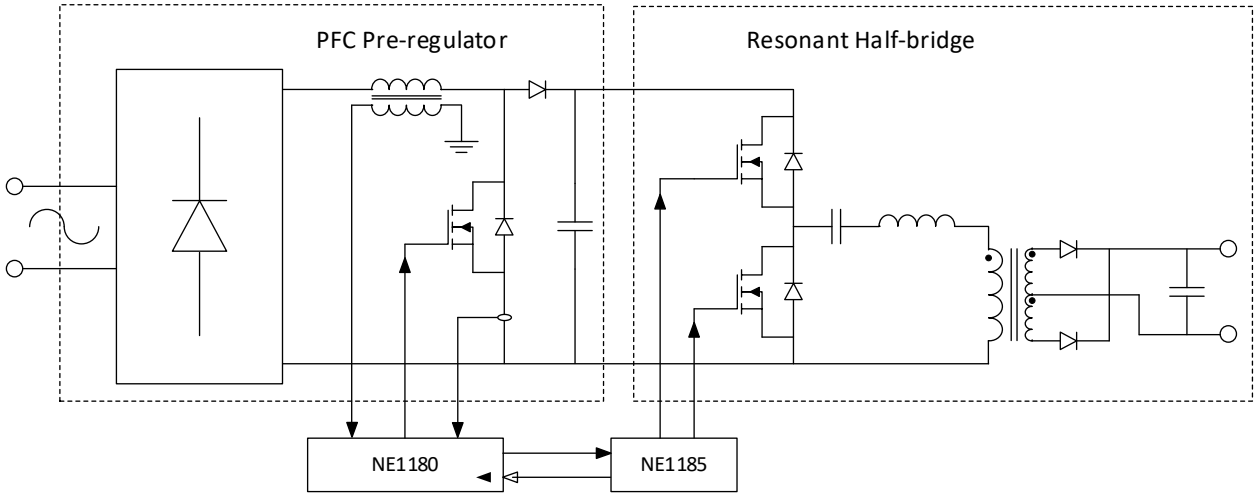
Features

- 50% Duty Cycle, Variable Frequency Control For Resonant Half-Bridge Converter
- 600V High-Side Gate Driver with Integrated Bootstrap Diode and High dV/dt Immunity
- 1A/2A Source/Sink Capability for Both High-Side and Low-Side Gate Drivers
- High-Accuracy Oscillator
- Operates at up to 600kHz
- Two-Level Over-Current Protection: Frequency-Shift and Latched Shutdown with Programmable Duration Time
- Remote ON/OFF Control and Brown-Out Protection through the BO Pin
- Latched-Disable Input for Easy Protections Implementation
- Interfaces with PFC Controller
- Programmable Burst-Mode Operation at Light-Load
- Non-Linear Soft-Start for Monotonic Output Voltage Rise
- SOP-16 package

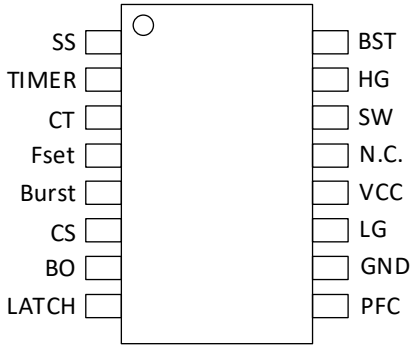
Features

- LCD and PDP TVs
- Desktop PCs and Servers
- Telecom SMPS
- AC-DC Adapter, Open-Frame SMPS
- Video Game Consoles
- Electronic Lighting Ballast

Typical Application



Pin Configuration



SOP-16

Functional Pin Description

Name	Pin	Description
SS	1	Soft-start. Connect an external capacitor with this pin to GND and a resistor to Fset pin to set the maximum oscillator frequency and the time constant for the frequency shift during start-up. An internal switch discharges the capacitor when the chip turns off (VCC < UVLO, VCC > 16V, BO < 1.25V or > 6V, LATCH > 1.85V, CS >1.5V, TIMER > 2V, thermal shutdown) to guarantee soft-start when the current sense pin voltage exceeds 0.8V, and as long as it stays above 0.75V.
TIMER	2	Period between over-current and shutdown. Connect a capacitor and a resistor from this pin to GND to set both the maximum duration from an over-current condition before the IC stops switching, and the delay before the IC resumes switching. Each time the CS pin voltage exceeds 0.8V, an internal 130μA source charges the capacitor; an external resistor slowly discharges this capacitor. If the pin voltage reaches 2V, the soft-start capacitor discharges completely, pushing the switching frequency to its maximum value; the 130uA source remains on. When the voltage exceeds 3.5V the IC stops switching and the internal current source turns off so that the pin voltage decays. The IC enters soft-started when the voltage drops below 0.3V. This allows the converter to work intermittently with very low average input power under short-circuit conditions.
CT	3	Time-Set. An internal current source programmed by the external network connected to pin 4 charges and discharges a capacitor connected to GND. Determines the converter's switching frequency.
FSET	4	Switching Frequency Set. Provides a precise 2V reference. A resistor connected from this pin to GND defines a current that sets the minimum oscillator frequency. Connect the phototransistor of an opto-coupler to this pin through a resistor to close the feedback loop that modulates the oscillator frequency to regulate the converter output voltage. The value of this resistor will set the maximum operating frequency. An R-C series connected from this pin to GND sets frequency shift at start-up to prevent excessive energy inrush (soft-start).
Burst	5	Burst-Mode Operation Threshold. The pin senses some voltage related to the feedback control, which is compared to an internal reference (1.25V). If the voltage on the pin is lower than the reference, the IC enters an idle state and reduces its quiescent current. The chip resumes switching when the voltage exceeds the reference by 50mV. Soft-start is not invoked. This function enables burst-mode operation when the load falls below a programmed level, determined by connecting an appropriate resistor to the opto-coupler to pin Fset (see block diagram). Tie the pin to Fset if burst-mode is not used.
CS	6	Primary-Current Sense. Uses a sense resistor or a capacitive divider to sense the primary current. The voltage signal requires an averaging filter because this input is not intended for cycle-by-cycle control. As the voltage exceeds a 0.8V threshold (with 50mV hysteresis), the soft-start capacitor on pin 1 discharges internally: The frequency increases, limiting the power throughput. Under an output short circuit, this normally results in a nearly-constant peak-primary current. A timer set on pin 2 limits the duration of this condition. If the current continues to build up despite the frequency increase, a second comparator referenced at 1.5V latches the device off and brings its consumption up to about pre-start-up levels. The information is latched, requiring cycling the IC supply voltage to restart: The latch is removed as the VCC voltage drops below the UVLO threshold. Tie the pin to GND if the function is not used.

BO	7	Input Voltage Sense. Connect to the high-voltage input bus through the tap of a resistor divider to perform either AC or DC (in systems with PFC) brownout protection. A voltage below 1.25V shuts down (without latching) the IC, lowers its consumption and discharges the soft-start capacitor. The IC operation resumes (with soft-start) when the voltage exceeds 1.25V. The comparator has current hysteresis: An internal 12µA current source is ON as long as the applied voltage is below 1.25V, and is OFF if this value is exceeded. Bypass the pin with a capacitor to GND to reduce noise pick-up. An internal Zener diode top-limits the pin voltage. Activating the Zener diode causes the IC to shut down (without latching). Bias the pin between 1.25V and 5.5V if the function is not used.
LATCH	8	IC Latch. Connects internally to a comparator that—when the pin voltage exceeds 1.85V—shuts the IC down and brings its consumption to near pre-start-up levels. The latch is removed as the VCC voltage goes below the UVLO threshold. Tie the pin to GND if the function is not used.
PFC	9	Interface to the front-end PFC. This pin—normally high—stops the PFC controller for protection purposes or during burst-mode operation. It goes low when the IC shuts down from the following conditions: VCC > 16V, LATCH > 1.85V, CS > 1.5V, BO > 5.5V, thermal shutdown and BURST < 1.25V. The pin also goes low when the voltage on TIMER exceeds 2V, and goes back open as the voltage falls below 0.3V. During UVLO, it is open. Leave the pin unconnected if not used.
GND	10	Ground. Current return for both the low-side gate-driver current and the IC bias current. Tie all bias component ground connections to a trace to this pin. Keep separate from any pulsed current return.
LG	11	Low-Side Gate Driver. The driver is capable of a minimum 0.9A source and a minimum 1.5A sink-peak current to drive the lower MOSFET of the half-bridge leg. The pin is actively pulled to GND during UVLO.
VCC	12	Supply Voltage. Supplies both the IC signal and the low-side gate driver. Sometimes a small bypass capacitor (e.g., 0.1µF) can help provide a clean bias voltage for the IC signal.
N.C.	13	High-Voltage Spacer. Not internally connected—isolates the high-voltage pin and eases compliance with safety regulations (creepage-distance) on the PCB.
SW	14	High-Side Switch Source. Current return for the high-side gate-drive current. Requires careful layout to avoid large spikes below ground.
HG	15	High-Side Floating Gate-Driver. Capable of minimum 0.9A source and minimum 1.5A sinkpeak current to drive the upper MOSFET of the half-bridge leg. An internal resistor connected to pin 14 (SW) ensures that the pin does not floating during UVLO.
BST	16	High-Side Gate Driver for Floating Voltage Supply. Connect a bootstrap capacitor between this pin and pin 14 (SW)—fed by an internal bootstrap diode driven in-phase with the lowside gate-drive.

Ordering Information

Product model	Packaging form	Logo	Smallest packaging
NE1185	SOP-16	NE1185	3000PCS

Absolute Maximum Ratings

Symbol	Pin	Parameter	Min.	Max.	Unit
V_{BST}	16	Floating supply voltage	-0.3	618	V
V_{SW}	14	Floating ground voltage	-0.3	V_{BST} - 18	V
dV_{SW}/dt	14	Floating ground max. slew rate	-0.3	50	V
VCC	12	IC supply voltage (ICC<25mA)	-0.3	Self-limited	V
V_{PFC}	9	Maximum voltage (pin open)	-0.3	VCC	V
I_{PFC}	9	Maximum sink current (pin low)	-0.3	Self-limited	V
I_{Fset}	4	Maximum source current	0.13	2	mA
LG	11	Maximum voltage	-0.3	VCC	V
	1-8	Analog inputs and outputs	-0.3	6	V
R_{IC}		Continuous power dissipation (TA = +25°C)		1.56	°C/W
T_J		Operating Junction Temperature	-40	150	°C
T_{STG}		Storage Temperature Range	-55	150	°C
T_L		Lead Temperature (Wave Soldering or R, 10Seconds)		260	°C
ESD		Human Body Model, JEDEC:JESD22-A114		2.5	KV
		Machine Model, JEDEC:JESD22- A115		250	V

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended period may affect device’s reliability.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	13	15.5	V
T_A	Operating Ambient Temperature	-40	125	°C
V_{IO}	Analog inputs and outputs	-0.3	6.5	V

Electrical Characteristics

Tj = 25°C, VCC = 13V, C_{HG} = C_{LG} = 1nF, CT = 470Pf, R_{Fset} = 12KΩ, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
IC supply voltage (VCC)						
V_{CC_Work}	VCC operating range		8.9		15.5	V
V_{CCH}	VCC high threshold, IC switch-on		10.2	10.9	11.6	V
V_{CCL}	VCC low threshold, IC switch-off		7.5	8.2	8.9	V
V_{hys}	Hysteresis			2.5		V
I_{clamp}	VCC clamp current during fault condition	VCC = 16.5V, LATCH = 2V		6		mA
V_{clamp}	VCC clamp voltage during fault condition	VCC < 16V or V_{LATCH} > 1.85V or V_{CS} > 1.5V or V_{TIMER} > 3.5V or V_{BO} < 1.25V or V_{BO} > 5.5V or OTP		15.2		V
IC supply current (VCC)						
$I_{start-up}$	Start-up current	Before the device turns on, V_{CC} = V_{CCH} - 0.2V		280	300	uA
I_q	Quiescent current	Device on, V_{Burst} = 1V		1	1.5	mA
I_{op}	Operating current	Device on, V_{Burst} = V_{Fset}		3	5.5	mA
I_r	Residual consumption	VCC < 8V or V_{LATCH} > 1.85V or V_{CS} > 1.5V or V_{TIMER} > 3.5V or V_{BO} < 1.25V or V_{BO} > 5.5V or OTP		250	400	uA
High-side floating-gate-driver supply (BST, SW)						
I_{LKBST}	BST pin leakage current	V_{BST} = 600V			50	uA
I_{LKSW}	SW pin leakage current	V_{SW} = 582V			50	uA
I_{CS}	Input bias current	V_{CS} = 0 to $V_{CSlatch}$			1	uA
t_{LEB}	Leading-edge blanking			250		ns
V_{CSx}	Frequency shift threshold		0.75	0.8	0.85	V
$V_{CSlatch}$	Latch-off threshold		1.41	1.5	1.59	V
Line voltage sensing (BO)						
V_{th}	Threshold voltage		1.2	1.25	1.3	V
V_{clamp}	Clamp level		5.5	6	6.5	V
I_{Hyst}	Current Hysteresis	VCC > 5V, V_{BO} = 0.3V	11	12	13	uA
Latch function (LATCH)						
I_{LATCH}	Input bias current	V_{LATCH} = 0 to V_{th}			1	uA
V_{th}	LATCH threshold		1.75	1.85	1.95	V
Oscillator						
D	Output duty cycle		48	50	52	%
f_{OSC}	Oscillation frequency				600	kHZ
t_D	Dead-time		300	320	350	ns
V_{CFp}	CT peak value			3.8		V
V_{CFv}	CT valley value			0.9		V
V_{REF}	Voltage reference at Fset pin		1.92	2	2.08	V

PFC function (PFC)						
V_L	Low saturation level	I_{PFC} = 1mA, V_{LATCH} = 2V			0.25	V
Soft start function (SS)						
R	Discharge resistance	$V_{CS} > V_{CSx}$		200		Ω
Standby function (Burst)						
V_{th}	Disable threshold		1.2	1.25	1.3	V
V_{hys}	Hysteresis			85		mV
Delayed shutdown (TIMER)						
I_{CHARGE}	Charge current	V_{TIMER} = 1V, V_{CS} = 0.85V	80	123	180	uA
V_{th_Fmax}	Threshold for forced operation at maximum frequency		1.9	2	2.1	V
V_{th_off}	Shut down threshold		3.3	3.5	3.7	V
$V_{th\_restart}$	Restart threshold		0.25	0.3	0.35	V
Low-side gate driver (LG, referenced to GND)						
$I_{sourcepk}$	Peak source current		1			A
I_{sinkpk}	Peak sink current		2			A
R_{source}	Sourcing resistor			10		Ω
R_{sink}	Sinking resistor			4		Ω
t_f	Fall time			12		ns
t_r	Rise time			20		ns
High side gate driver (HG, referenced to SW)						
$I_{sourcepk}$	Peak source current		1			A
I_{sinkpk}	Peak sink current		2			A
R_{source}	Sourcing resistor			10		Ω
R_{sink}	Sinking resistor			4		Ω
t_f	Fall time			10		ns
t_r	Rise time			20		ns
Thermal Shutdown						
$T_{shutdown}$	Thermal shutdown threshold			150		℃
$T_{recovery}$	Thermal shutdown recovery threshold			127		℃

Block Diagram

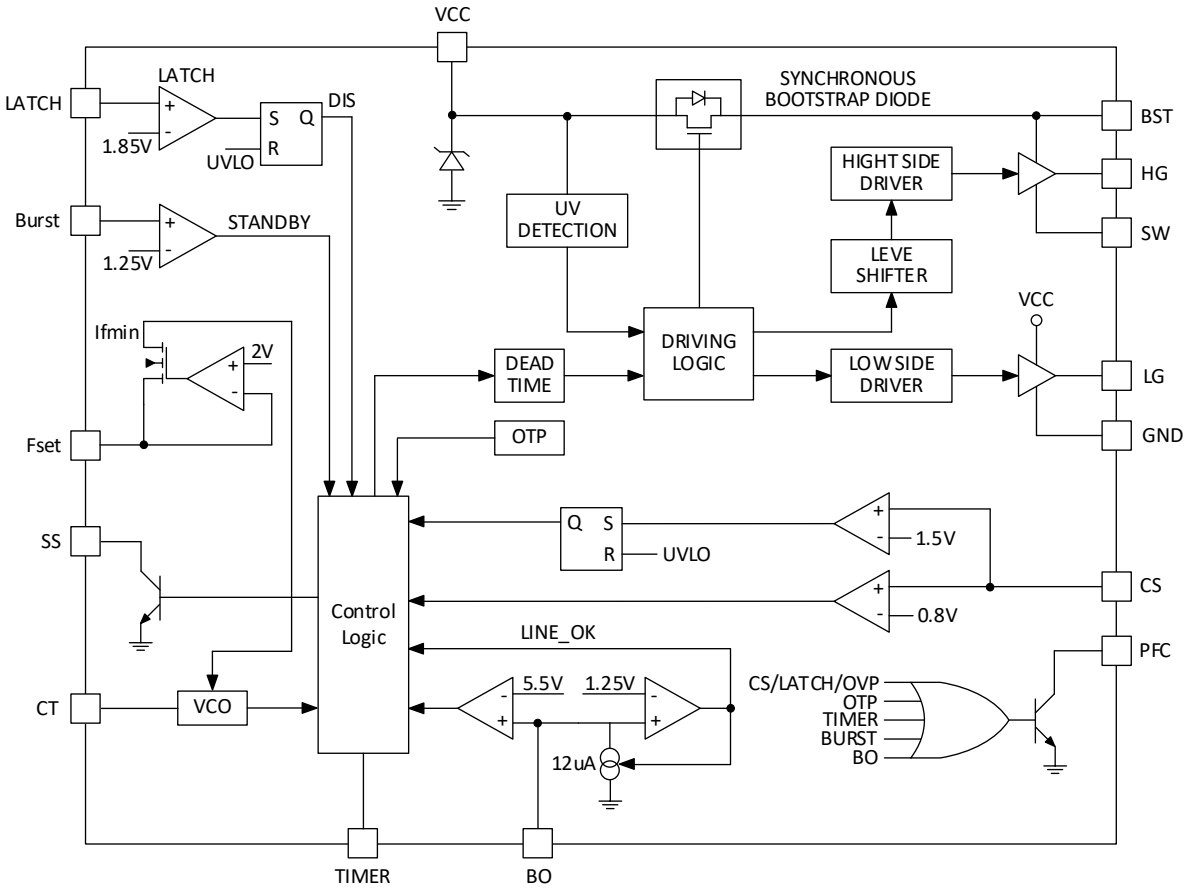


Figure 1. Functional Block Diagram

Functional Description

Oscillator

The charge/discharge time of the CT capacitor determines the oscillator frequency. The voltage on the CT capacitor fluctuates between the peak threshold and valley threshold to form a triangle waveform. Figure 2 shows the detailed waveform during steady state.

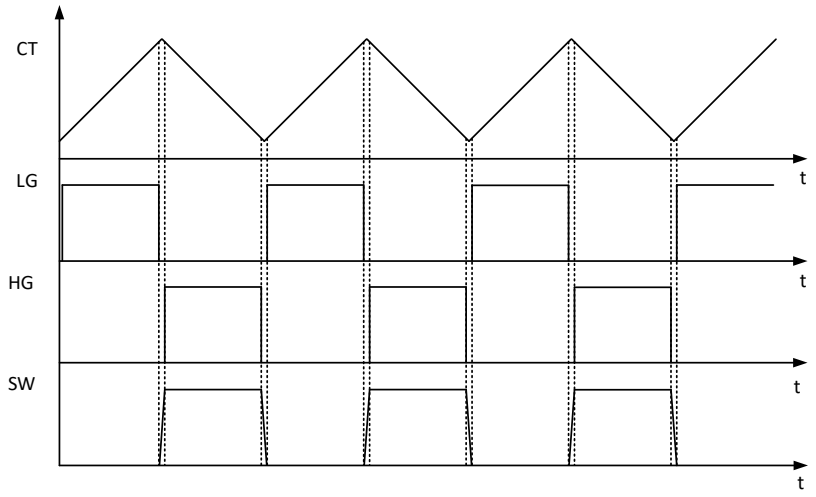


Figure 2. CT Waveform and Gate Signal

The network connecting the Fset pin charges/discharges the current on the CT capacitor, as Figure 3 shows. The source current of the Fset pin controls the current source-1 (I_{S-1}) to charge the CT capacitor. When a switching cycle starts, I_{S-1} charges the CT capacitor until the voltage triggers the peak threshold voltage. Then the discharge current source (I_{S-2}) with twice the source current of the Fset pin turns on. Therefore, the CT capacitor discharges with the source current of the Fset pin. When the voltage on the CT capacitor drops to the valley threshold voltage, the I_{S-2} turns off and then a new switching cycle is enabled.

Based on the block diagram shown in Figure 3, the Fset RC network functions as described:

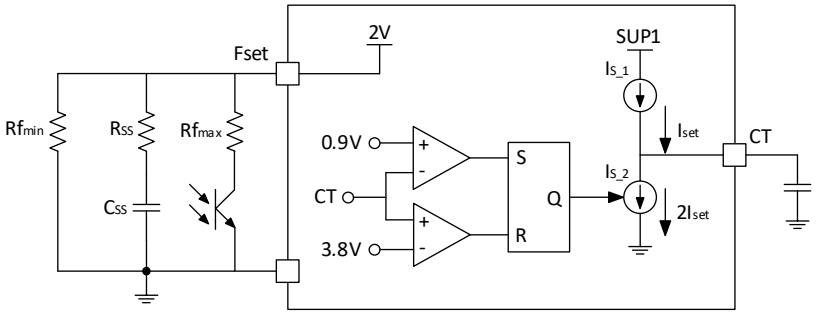


Figure 3. Oscillator Block Diagram

1. Rf_{min} from the Fset pin to GND sets the maximum resistance of external RC network when the phototransistor is blocked, therefore setting the Fset minimum source current, which sets the minimum switching frequency;
2. Under normal operation, the phototransistor modulates the current flow through Rf_{max} to modulate the frequency for output voltage regulation. When the phototransistor is saturated, the current flow through Rf_{max} is at its maximum, setting the frequency at its maximum
3. A series RC circuit connected between Fset and GND determines the frequency shift at start-up. (Please see the soft-start section for details.)

Based on the previous principles, the following equations describe the minimum and maximum frequency:

$$f_{min} = \frac{1}{3 \times CT \times Rf_{min}}$$

$$f_{max} = \frac{1}{3 \times CT \times (Rf_{min} \| Rf_{max})}$$

Typically, the CT capacitance is between 0.1nF and 1nF, so the values of Rf_{min} and Rf_{max} are:

$$Rf_{min} = \frac{1}{3 \times CT \times f_{min}}$$

$$Rf_{max} = \frac{Rf_{min}}{\frac{f_{max}}{f_{min}} - 1}$$

For the CT capacitance selection, here is a note for low temperature and high switching frequency application: when the temperature is low, the source current capability of Fset pin drops a little due to the property of internal transistor circuit, which means there might be not big enough current to charge/discharge the large CT capacitor. So a small CT cap (<=330pF) is recommended for such application.

Burst-Mode Operation

Under light-load or in the absence of a load, the maximum frequency limits the resonant half-bridge switching frequency. To control the output voltage and limit power consumption, the NE1185 can enable compatible converters to operate in burst-mode to sharply reduce the average switching frequency, thus reducing the average residual magnetizing current and the associated losses.

Operating in burst-mode requires setting the Burst pin on the NE1185; if the voltage on the Burst pin drops below 1.25V, NE1185 will shut down the HG and LG gate drive outputs, leaving only the 2V reference voltage on the Fset pin and the SS pin to retain the previous state and minimize NE1185's power consumption. When the voltage on the Burst pin exceeds 1.25V by 50mV, NE1185 resumes normal operation.

Based on the Burst-mode operating principle, the Burst pin voltage must connect to the feedback loop. Figure 4 shows a typical circuit connect the Burst pin to the feedback signal for narrow-input–voltage range applications:

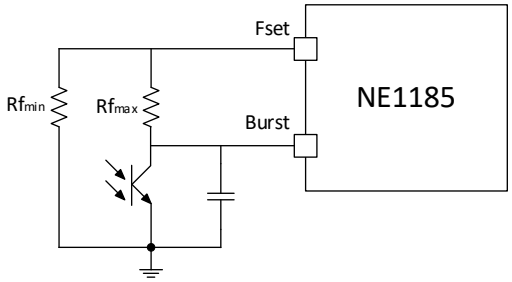


Figure 4. Bust-Mode Operation Set-Up

In addition to setting the oscillator, Rf_{max} also determines the maximum switching frequency that NE1185 operates in burst-mode. After confirming f_{max}, calculate Rf_{max} as below:

$$Rf_{max} = \frac{3}{8} \times \frac{Rf_{min}}{\frac{f_{max}}{f_{min}} - 1}$$

Here, f_{max} corresponds to a load point, P_{Burst}, where the peak current flow through the transformer is too low to cause audible noise.

The above introduction is based on a narrow input voltage range. As a property of the resonant circuit, input voltage also determines the switching frequency. That means the P_{Burst} has a large variance over the wide input voltage range. To stabilize P_{Burst} over the input range, use the circuit in Figure 5 to insert the input voltage signal into feedback loop.

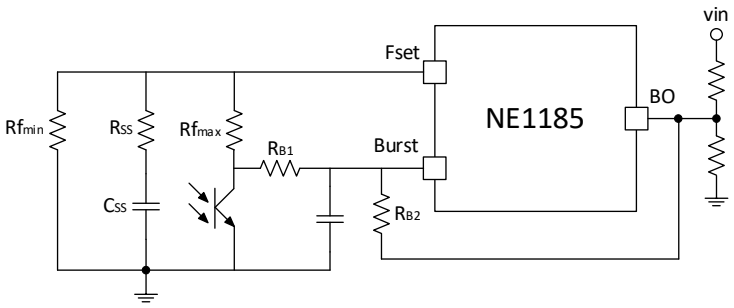


Figure 5. Bust-mode Operation Set-up for Wide Input Voltage Range

R_{B1} and R_{B2} from Figure 5 correct against the wide input voltage range. Select both resistors based on experimental results. Note that the total resistance of R_{B1} and R_{B2} should be much bigger than RH to minimize the effect on the BO pin voltage. During burst-mode operation, when the load is lower than P_{Burst}, the switching frequency is clamped at the maximum frequency. Then the output voltage must rise over the set value, which would increase the current flowing through the opto-coupler. Therefore, the voltage on Rf_{max} must rise due to the increased opto-transistor current. The Burst pin voltage would then drop below 1.25V, triggering the gate signal OFF state. Until the output voltage falls below the setting value, the current flow through opto-coupler then decreases, causing the Burst pin voltage to rise. When the voltage exceeds 1.25V+100mV, the IC restarts to generate the gate signal. The IC will continue to operate in this mode under no-load or light-load to decrease average power consumption.

PFC-Disable Function

Many applications require a PFC function, making a pre-regulator widely before a resonant circuit common. Under some conditions—e.g. no-load or light load, OCP, OVP—require disabling the PFC.

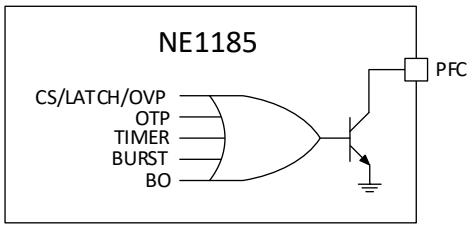


Figure 6. NE1185 and the PFC controller

The NE1185 provide PFC disabling. Pull the PFC pin low for one of following conditions:

- gate-off during burst-mode (Burst < 1.25V);
- OCP (CS > 1.5V); input over-voltage (BO > 5.5V);
- Latch pin HIGH (Latch > 1.85V);
- TIMER pin voltage exceeding 2V without dropping to 0.3V;
- over-temperature protection triggering.

Shutdown the PFC to reduce power consumption or to protect the system. Figure 6 shows the typical application circuit between the NE1185 and the PFC controller.

If this function is not used, PFC pin can float.

Soft-Start Operation

For the resonant half-bridge converter, the power delivered is inversely proportional to the switching frequency. To achieve soft-start, start the switching frequency with a high value until the value is controlled by the closed loop.

The converter + NE1185 can easily achieve soft-start using an external RC series circuit as shown in Figure 7.

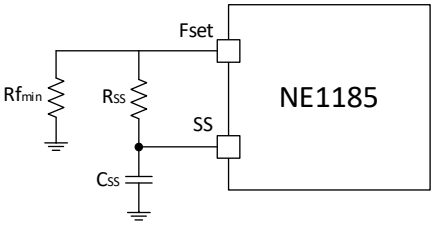


Figure 7. Soft-Start Block

When start-up begins, the SS voltage is 0V, so the soft-start resistor (R_{SS}) is in parallel to Rf_{min}: Rf_{min} and R_{SS} determine the initial frequency as:

$$f_{start} = \frac{1}{3 \times CT \times (Rf_{min} \| R_{SS})}$$

During start-up, the C_{SS} charges until its voltage reaches the reference–2V, and the current flow through R_{SS} drops to zero. This period takes about $5(R_{SS} \times C_{SS})$. During this period, the switching frequency changes following an exponential curve: the C_{SS} charge initially decays relatively quickly but the rate progressively slows.

After this period ends, the output voltage is not still close to the setting value, so the feedback loop will take over start-up. With soft-start, the input current increases gradually until the output voltage reaches the setting point with little overshoot. Select the soft-start RC network as per the equations below:

$$R_{SS} = \frac{Rf_{min}}{\frac{f_{start}}{f_{min}} - 1}$$

$$C_{SS} = \frac{3 \times 10^{-3}}{R_{SS}}$$

Select an initial frequency, f_{start}, at least 4×fmin. Select C_{SS} as a trade-off between the desired soft-start operation and the OCP speed (see the next section for details).

Current Sensing

Figure 8 shows the current sense block diagram.

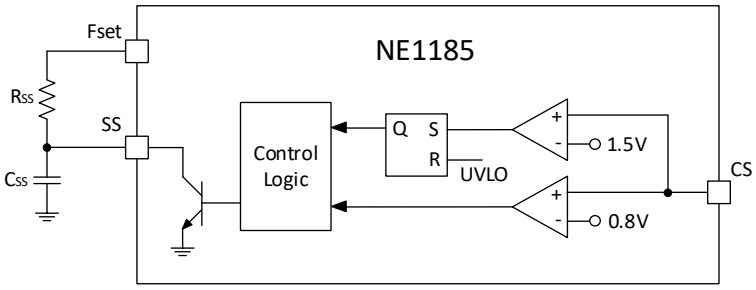


Figure 8. Current Sensing Block Diagram

There are two levels over-current protection.

The first level occurs when the CS voltage exceeds 0.8V, the comparator triggers the control logic to output a high-level control signal that turns on the transistor connecting SS and GND. Then the C_{SS} voltage drop results a sharp increase in oscillator frequency, and therefore reduces the energy transferred to the output. When the CS pin voltage drops back to 0.79V, the converter resumes normal operation with the help of the 10mV hysteresis.

Generally, the CS pin voltage continues to rise during a short circuit. The second level overcurrent protection triggers when the CS pin voltage rises to 1.5V. Then the IC is latched at very low consumption (residual consumption in EC table).

For two-level protection, a very large C_{SS} slows the discharge to the point that the transformer and the resonant inductor saturate and damages the secondary diode.

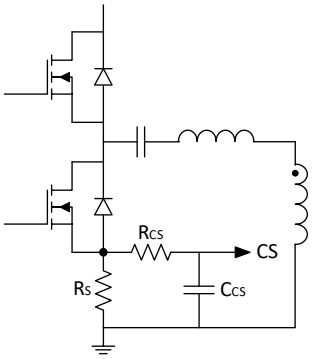


Figure 9. Current Sensing with a Sense Resistor

There are two types of current sensing methods: one uses a sense resistor in series with the low side MOSFET; the other uses a lossless current-sensing network. The first method is simple but causes some unnecessary power consumption.
Calculate the sense resistor using the following equation:

$$R_S = \frac{4}{I_{Crpk}}$$

Where I_{Crpk} is the desired peak current through the primary MOSFET for the resonant capacitor at low input voltage and full load.
Since the circuit require an RC filter between the sensing resistor and CS pin, select an RC time constant at around $10/f_{min}$.

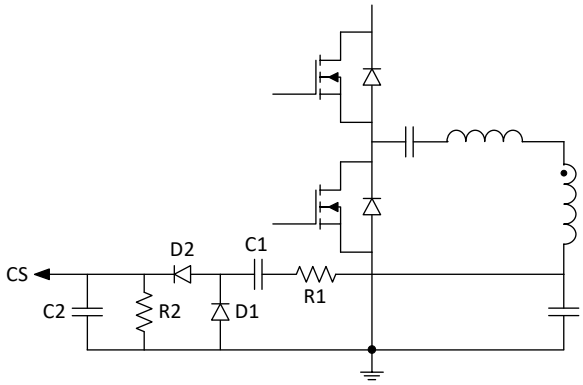


Figure 10. Current Sensing with Lossless Network

To design the lossless current sensing network, consider these two conditions:

1. R1 is smaller than several hundred ohms. The sensing network acts as a capacitive current divider. Use the equations below:

$$C1 \leq \frac{Cr}{100}$$

$$R2 = \frac{0.8 \times \pi}{I_{Crpk}} \times \left(1 + \frac{Cr}{C1}\right)$$

2. R1 is ~10kΩ. The sensing network acts to divide the ripple voltage on Cr. Design for this condition as per the equations below:

$$C1 \leq \frac{Cr}{100}$$

$$R2 = \frac{0.8 \times \pi}{I_{Crpk}} \times \frac{\sqrt{R1^2 + {X_{C1}}^2}}{X_{C1}}$$

Calculating the reactance of C1 and Cr at the frequency where the maximum peak resonant current occurs. Empirically, the R2 and C2 time constant is about $10/f_{min}$.
Depending on the circuit, consider the calculated value as a cut value that requires adjustments based on experimental results to meet the design target.
The OCP can limit the energy transferred from the primary to the secondary during over-load or short-circuit period.

However, excessive power consumption due to high continuous currents can damage the secondary-side windings and the rectifiers. The NE1185 provides additional protection to reduce the average power consumption during OCP: When OCP triggers, the converter enters a hiccup-like protection mode that operates intermittently.

Set the maximum over-load or short circuit operating time (t_{OC}) by selecting appropriate C_{Timer} and R_{Timer}. During the first OCP level when the CS voltage exceeds 0.8V, an internal 130μA current source turns on to charge C_{Timer}. When the voltage on C_{Timer} reaches 2V, the C_{SS} voltage drops below the OCP comparator output. This forces the switching frequency to equal f_{start} to minimize the transferred energy. t_{OC} is the time for the voltage on C_{Timer} to rise from 0V to 2V. However, there is no simple relationship between t_{OC} and C_{Timer}. Select C_{Timer} based on experimental results (based on experiments: C_{Timer} may increase operating time by 100ms).

After the voltage on C_{Timer} rises to 2V, the 130uA current source continues to charge it until the voltage reaches the shutdown threshold (3.5V). This period is approximately:

$$t_{OP} = 10^4 \times t_{Timer}$$

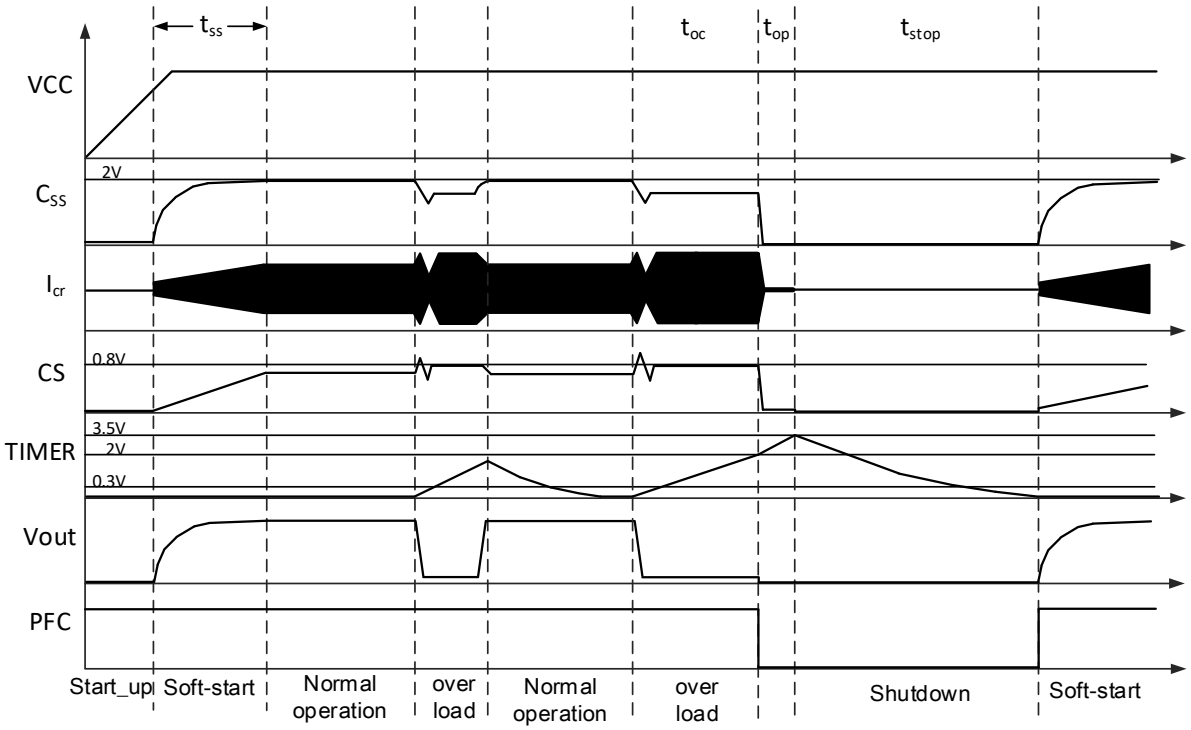


Figure 11. Delayed Shutdown and Soft-start Time Sequence

During this period, the switching frequency remains at f_{start} to limit the energy transferred. When the shutdown threshold triggers, the gate drive turns off and the 130μA current source shuts down. Then R_{Timer} slowly discharges C_{Timer}. This procedure lasts until the C_{Timer} voltage drops below 0.3V, then the IC restarts. This time period is:

$$t_{OFF} = R_{Timer} \times C_{Timer} \times ln\frac{3.5}{0.3} \approx 2.5R_{Timer} \times C_{Timer}$$

Figure 11 shows the operation's time sequence.

Latch Operation

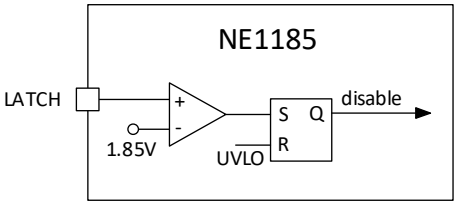


Figure 12. Latch Function Block

The NE1185 provides a simple latch-off function through the Latch pin. Applying an external voltage > 1.85V causes the IC to enter a latched shutdown. After IC is latched, its consumption drops, as shown by the residual current in the EC table. Resetting the IC requires dropping the VCC voltage below the UVLO threshold.

Input Voltage Sensing

The NE1185 can stop when the input voltage drops below a specified value, and then restarted when the input voltage goes back to normal. This function guarantees that the resonant half-bridge converter always operates within the specified input voltage range. The IC senses voltage on BO through the tap of a resistor divider connected to the rectified AC voltage or the PFC output.

Figure 13 shows the line-sensing internal block diagram.

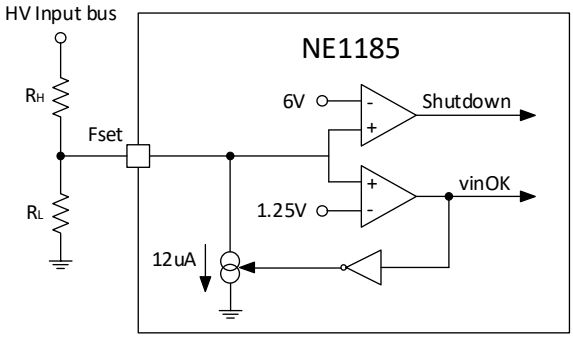


Figure 13. Input Voltage Sensing Block

The internal 12μA current source turns on when the BO voltage drops below 1.25V, and turns off when the BO voltage exceeds 1.25V. When the BO voltage drops below 1.25V, the IC shuts down the gate drive, and consumes very little power as per the residual current in the EC table. Calculate the input-voltage resistor divider with the desired ON (Vin_{ON}) and OFF (Vin_{OFF}) input voltage as below:

$$R_H = \frac{Vin_{ON} - Vin_{OFF}}{12 \times 10^{-6}}$$

$$R_L = R_H \times \frac{1.25}{Vin_{OFF} - 1.25}$$

For additional protection, when the BO voltage exceeds the internal 5.5V clamp voltage, the IC will shutdown. When the BO voltage is between 1.25V and 5.5V, the IC will restart.

High-Side Gate Driver

The external BST capacitor provides energy to the high-side gate driver. An integrated bootstrap diode charges this capacitor through VCC. This diode simplifies the external driving circuit for the high-side switch, allowing the BST capacitor to charge when the low side MOSFET is on.

To provide enough gate driver energy and considering the BST capacitor charge time, use a 100nF-to-1μF capacitor for the BST capacitor.

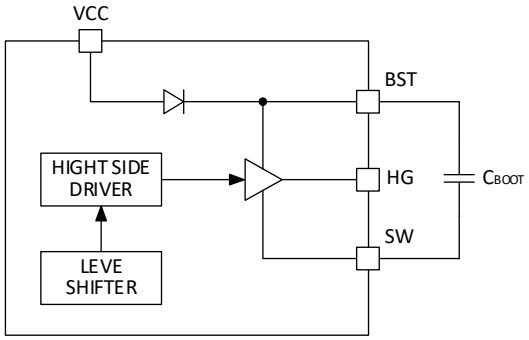


Figure 14. High-Side Gate Driver

Low-Side Gate Drive

The LG pin provides the gate driver signal for the low-side MOSFET. The maximum absolute rating table shows that the maximum LG pin voltage is 16V. Under some conditions, a large voltage spike occurs on the LG pin due to oscillations from the long gate-driver wire, the MOSFET parasitic capacitance, and the small gate-driver resistor. This voltage spike is dangerous to the LG pin, so add a 15V Zener diode close to the LG and GND pins.

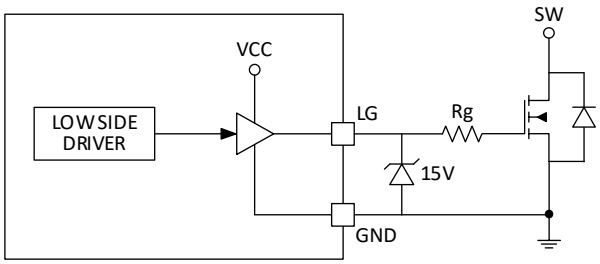


Figure 15. Low-Side Gate Driver

Layout Guideline

PCB layout is critical to the circuit normal operation, EMI performance, surge and thermal. So designer must pay attention to the layout guide as follows:

1. The loop of the main power flow should be as short as possible, and the wire should be as wide as possible.
2. Separate the power GND from the signal GND, try to connect the two GND at the minus of bulky capacitor.
3. The peripheral components from pin 1 to pin 8 shall be placed as close as possible to the corresponding pin.
4. The feedback wire from opto-coupler shall be rooted as close as possible to the IC and be far away from hot spot, like SW, HG etc.

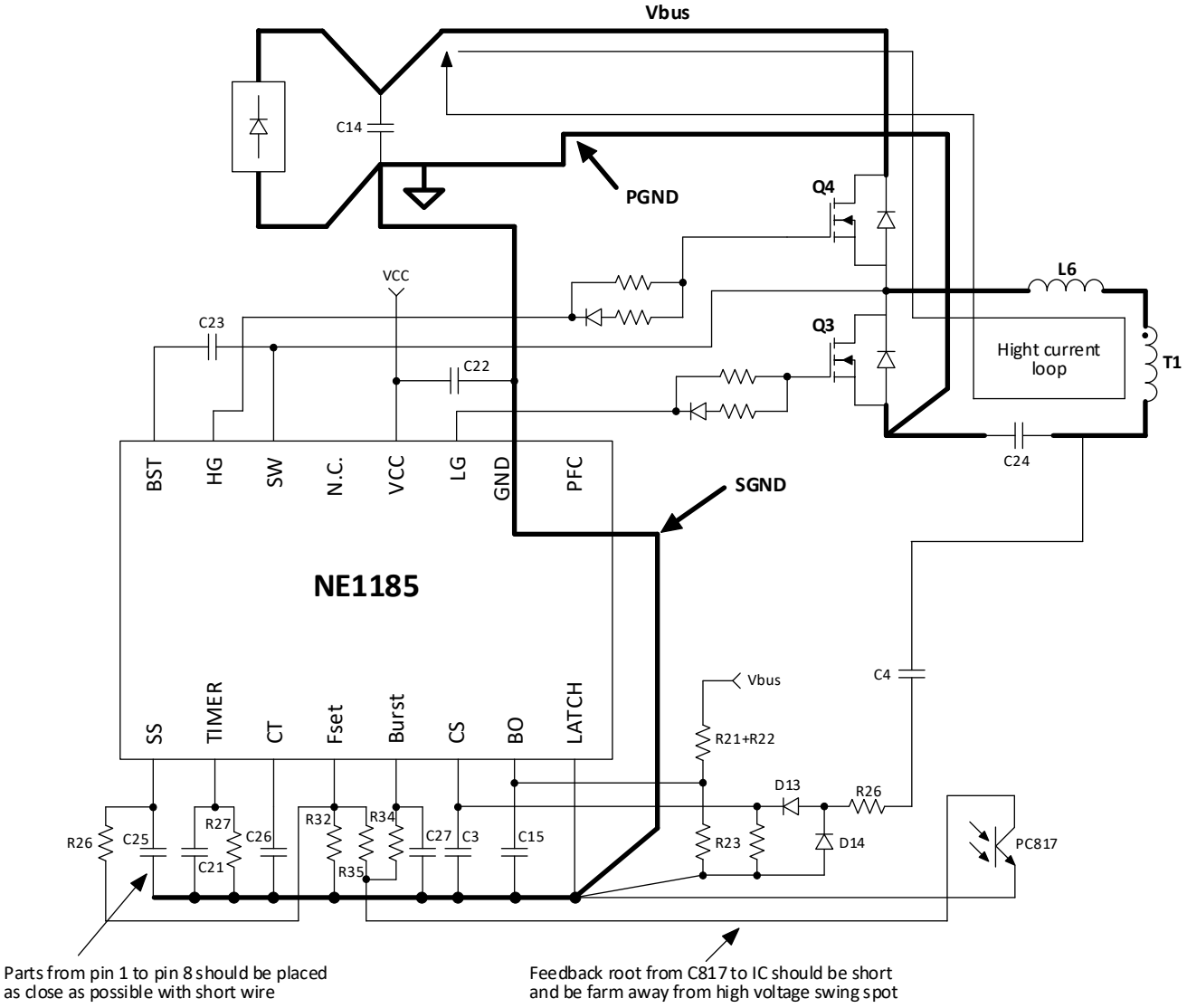
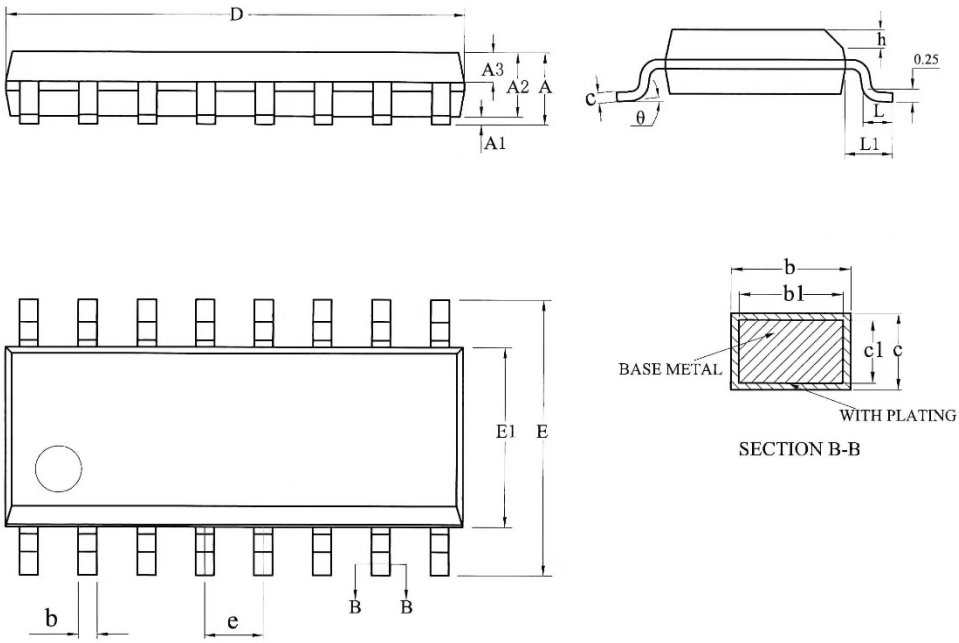


Figure 16. Key Notes for Layout Guideline

Package Information

SOP-16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

说明：

1. 所有标注尺寸单位均为毫米
2. 长度/宽度不包括封装毛边
3. 图纸不是按比例绘制的
4. 当从左到右读顶部标记时，Pin 1 在左下角