Description

NE1280 is a controller for Continuous Conduction Mode (CCM) Power Factor Correction step−up pre−converters. It controls the power switch conduction time (PWM) in a fixed frequency mode and in dependence on the instantaneous coil current.

NE1280 minimizes the number of external components and drastically simplifies the PFC implementation. It also integrates high safety protection features that make the NE1280 a driver for robust and compact PFC stages like an effective input power runaway clamping circuitry.

NE1280 permanently monitors the output voltage, the coil current and the die temperature to protect the system from possible over−stresses.

NE1280 offers comprehensive protection coverage UVLO, Soft Start, Over−Power Limitation, Overvoltage protection, coil current limitation, Brown−Out Detection, Over−Power Limitation, thermal shutdown.

NE1280 is offered in SOP-8 package.

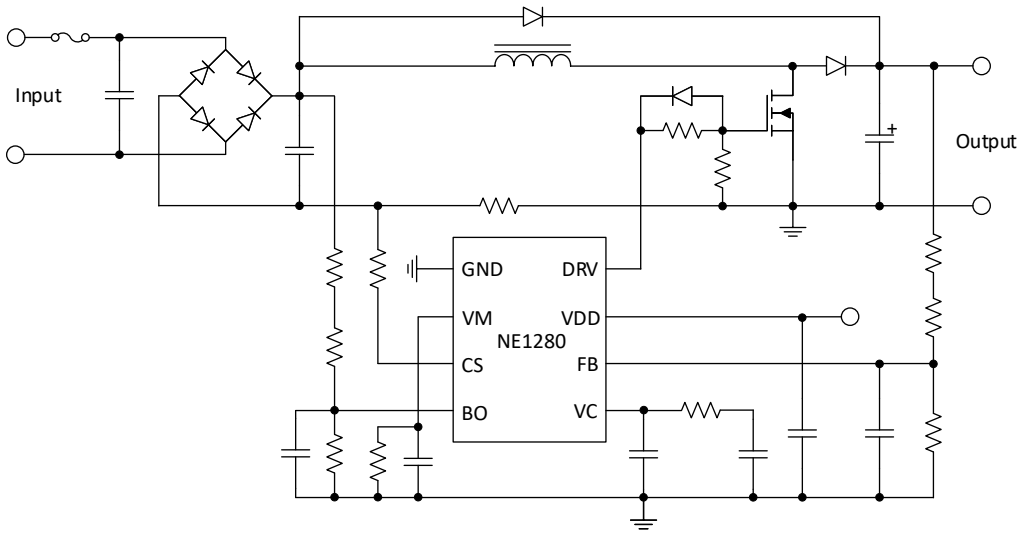
Features

- Average Current Continuous Conduction Mode
- Fast Transient Response
- Very Few External Components
- Low Startup Current and Shutdown Current
- ±1.5 A Totem Pole Gate Drive
- Low Operating Consumption
- Accurate Fully Integrated 65kHz and 130KHz Oscillator
- Soft−Start for Smoothly Startup Operation
- Undervoltage Detection for Open Loop Detection or Shutdown
- Overvoltage Protection
- Brown−Out Detection
- Over Temperature Protection (OTP)
- Accurate Overcurrent Limitation

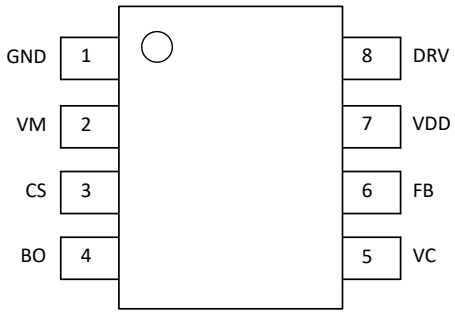
Applications

- AC Adapters
- Flat TVs, PC Desktops
- White Goods, other Off−line SMPS

Typical Application



Pin Configuration



SOP-8

Functional Pin Description

Name	Pin	Description
GND	1	Ground
VM	2	This pin provides a voltage V_M for the PFC duty cycle modulation. The device operates in average current mode if an external capacitor C_M is connected to the pin. Otherwise, it operates in peak current mode.
CS	3	This pin sources a current I_{CS} which is proportional to the inductor current I_L. The sense current I_{CS} is for overcurrent protection (OCP), overpower limitation (OPL) and PFC duty cycle modulation.
BO	4	Connect a resistor network among the rectified input voltage, BO pin, and ground. And connect a capacitor between BO pin and ground. BO pin detects a voltage signal proportional to the average input voltage. This signal which is proportional to the RMS input voltage Vac is also for overpower limitation (OPL) and PFC duty cycle modulation. The V_{BO} can also reach brown−out protection.
VC	5	The voltage of this pin VC directly controls the input impedance. This pin is connected to external type−2 compensation components to limit the VC bandwidth typically below 20Hz to achieve near unity power factor. When it starts operation, the power increases slowly (soft−start).
FB	6	This pin receives a feedback signal V_{FB} that is proportional to the PFC circuits output voltage. This information is used for both the output regulation, the overvoltage protection (OVP), and output undervoltage protection (UVP) to protect the system from damage at feedback abnormal situation.
VDD	7	This pin is the positive supply of the IC. After start−up, the operating range is 9V up to 28 V.
DRV	8	The high current capability of the totem pole gate drive (±1.5A) makes it suitable to effectively drive high gate charge power MOSFET.

Ordering Information

Part number	Package	Logo	Fosc	Smallest packaging
NE1280	SOP-8	NE1280	65KHz	4000PCS
NE1280A	SOP-8	NE1280A	130KHz	4000PCS

Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Power Supply Voltage, VDD pin, continuous voltage	-0.3	30	V
	Transient Power Supply Voltage, duration < 10ms, I_{VDD} < 10mA		29	V
V_{VM}	Input Voltage	-0.3	7	V
V_{CS}	Input Voltage	-0.3	7	V
V_{BO}	Input Voltage	-0.3	7	V
V_{VC}	Input Voltage	-0.3	7	V
V_{FB}	Input Voltage	-0.3	7	V
DRV	Output Drive Capability – Source		-1.5	A
	Output Drive Capability – Sink		+1.5	A
R_{JA}	SOP-8 Thermal Resistance (Junction-to-Air)		150	°C/W
T_J	Operating Junction Temperature	-40	125	°C
T_{STG}	Storage Temperature Range	-55	160	°C
T_L	Lead Temperature (Wave Soldering or IR,10Seconds)		260	°C
ESD	Human Body Model, JEDEC:JESD22-A114		2.5	KV
	Machine Model, JEDEC:JESD22- A115		250	V

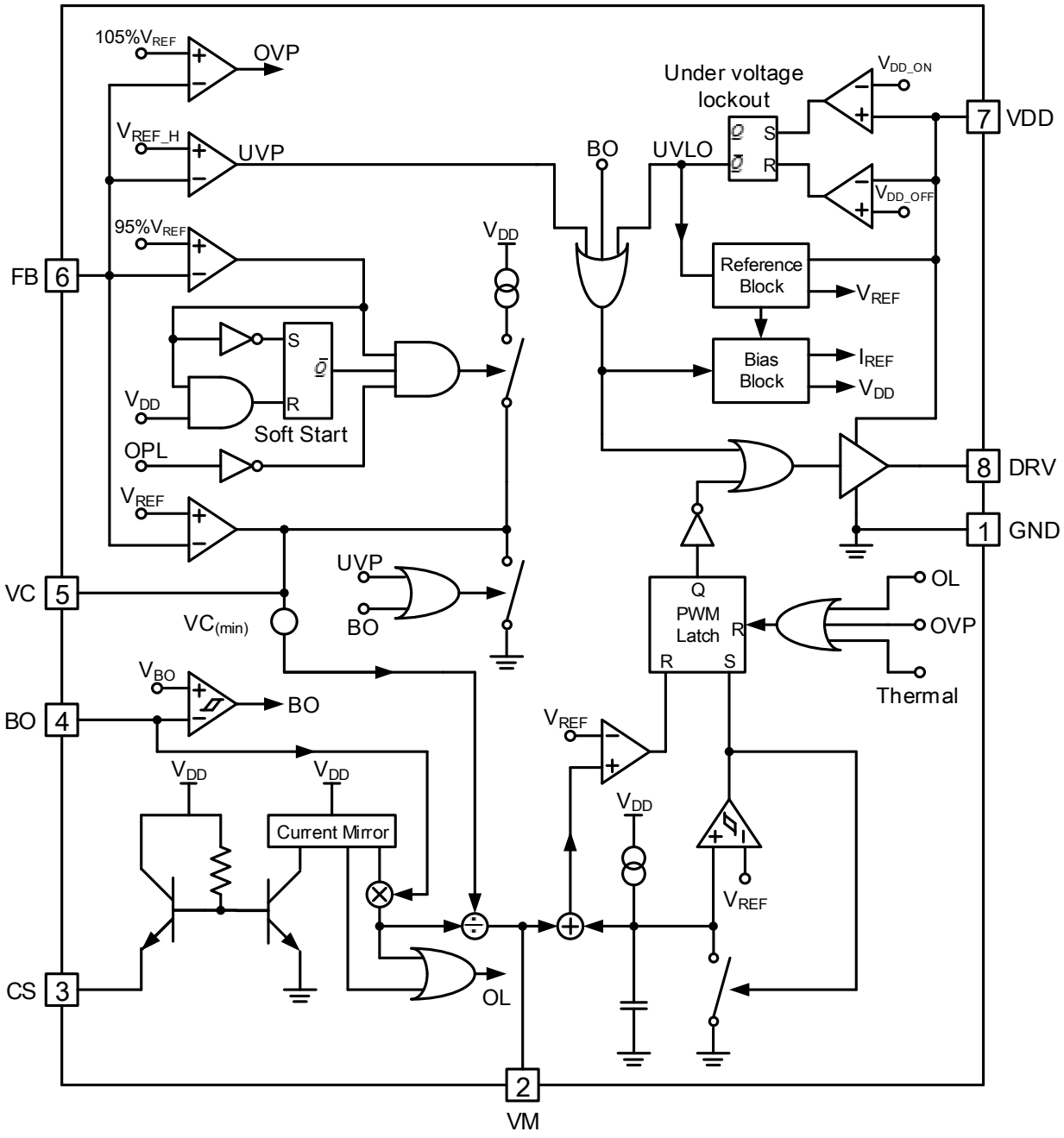
Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended period may affect device’s reliability.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage	10	28	V
T_A	Operating Ambient Temperature	-25	125	°C

Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sink, at 45°C ambient.Higher output power is possible with extra added heat sink or air circulation to reduce thermal resistance.

Block Diagram



Electrical Characteristics

(T_A = 25°C, V_{DD}=15V, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD Section						
I_{DD_ST}	Startup Current	VDD=9.9V			75	uA
I_{DD_OP1}	Operation Current	VDD=15V, no load, no switching		3.5	5.0	mA
I_{DD_OP2}	Operation Current	VDD=15V, no load, switching		4.5	6.0	mA
$I_{Shutdown}$	Shutdown Mode	VDD=15V,FB=0V		380	480	uA
V_{DD_ON}	Threshold Voltage to Startup	VDD Rising	10.0	10.8	11.5	V
V_{DD_OFF}	Threshold Voltage to Stop Switching in Normal Mode	VDD Falling	8.6	9.3	10.0	V
V_{DD_H}	Undervoltage Lockout Hysteresis		1.0	1.5		V
V_{DD_Clamp}	VDD Clamp voltage	I_{DD}=10mA		29.0		V
Regulation Section						
V_{REF}	FB Voltage Reference		2.425	2.50	2.575	V
I_{EA}	Error Amplifier Current Capability			±32		uA
G_{EA}	Error Amplifier Gain		100	200	300	uS
I_{FB}	FB Bias Current	$V_{FB} = V_{REF}$	-500		500	nA
$VC_{(max)}$	Maximum Control Voltage	V_{FB}=2.0V		3.6		V
$VC_{(min)}$	Minimum Control Voltage	V_{FB}=3.0V		0.6		V
ΔV_C	$VC_{(max)} - VC_{(min)}$		2.7	3.0	3.3	V
$V_{OUT}L / V_{REF}$	Ratio (V_{OUT} Low Detect Thresold / V_{REF})		94	95	96	%
$H_{OUT}L / V_{REF}$	Ratio (V_{OUT} Low Detect Hysteresis / V_{REF})			0.5		%
I_{BOOST}	VC Source Current when (V_{OUT} Low Detect) is activated		200	230	260	uA
Current Sense Section						
V_S	Current Sense Pin Offset Voltage	I_{CS} = 100uA		10		mV
I_{S_OCP}	Overcurrent Protection Threshold		185	200	215	uA
Power Limitation Section						
I_{CS} x V_{BO}	Overpower Limitation Threshold			200		uVA
I_{CS_OPL1}	Overpower Current Threshold	V_{BO} = 0.9V, V_M = 3V	180	220	305	uA
I_{CS_OPL2}	Overpower Current Threshold	V_{BO} = 2.67V, V_M = 3V	60	75	110	uA
Oscillator Section						
F_{OSC}	Switching Frequency (NE1280)		60	65	70	KHz
	Switching Frequency (NE1180A)		120	130	140	KHz
Dcycle	Duty Cycle Range			0-97		%

Brown−out Detection Section						
V_{BOH}	Brown−Out Voltage Threshold	rising	1.20	1.30	1.40	V
V_{BOL}	Brown−Out Voltage Threshold	falling	0.65	0.70	0.75	V
I_{IB}	BO Input Bias Current	V_{BO} = 1 V	-500	-	500	nA
Current Modulation Section						
I_{M1}	Multiplier Output Current	VC = VC (max), V_{BO} = 0.9 V, I_{CS} = 25 uA		2.0		uA
I_{M2}	Multiplier Output Current	VC = VC (max), V_{BO} = 0.9 V, I_{CS} = 75 uA		5.8		uA
I_{M3}	Multiplier Output Current	VC = VC (min) + 0.2 V, V_{BO} = 0.9 V, I_{CS} = 25 uA		29.0		uA
I_{M4}	Multiplier Output Current	VC = VC (min) + 0.2 V, V_{BO} = 0.9 V, I_{CS} = 75 uA		86.0		uA
Over Voltage Section						
V_{OVP} / V_{REF}	Ratio	Overvoltage Threshold / V_{REF}	103	105	107	%
T_{OVP}	Propagation Delay	(V_{FB} − 107% V_{REF}) to Drive Low		500		nS
Under Voltage Protection / Shutdown						
$V_{UVP(on)}/V_{REF}$	UVP Activate Threshold Ratio	T_J = 0°C to +105°C	4	8	12	%
$V_{UVP(off)}/V_{REF}$	UVP Deactivate Threshold Ratio	T_J = 0°C to +105°C	6	12	18	%
V_{UVP_H}	UVP Lockout Hysteresis			4		%
T_{UVP}	Propagation Delay	(V_{FB} < 8%V_{REF}) to Drive Low		500		nS
Thermal Shutdown						
T_{SD}	Thermal Shutdown Threshold		150			°C
H_{SD}	Thermal Shutdown Hysteresis			30		°C
Driver Section						
V_{OL}	Output Low voltage	Io=100mA			1.0	V
V_{OH}	Output High voltage	Io=100mA	6.0			V
$T_{\_r}$	Output Rise time	1.5V ~ 13.5V @ CL=2.2nF		60		ns
$T_{\_f}$	Output Fall time	13.5V ~ 1.2V @ CL=2.2nF		40		ns

Functional Description

NE1280 is a PFC driver designed to operate in fixed frequency, continuous conduction mode. The fixed frequency operation eases the compliance with EMI standard and the limitation of the possible radiated noise that may pollute surrounding systems. In addition, continuous conduction operation reduces the application di/dt and their resulting interference. More generally, NE1280 is an ideal candidate in systems where cost−effectiveness, reliability and high power factor are the key parameters.

NE1280 requires a minimum of external components. In particular, the circuit scheme simplifies the PFC stage design and eliminates the need for any input voltage sensing. In addition, the circuit offers some functions like the Brown−Out or the true power limiting that enable the optimizations of the PFC design.

NE1280 is optimized to exhibit consumption as small as possible in all operation modes. The consumed current is particularly reduced during the start−up phase and in shutdown mode so that the PFC stage power losses are extremely minimized when the circuit is disabled. This feature helps meet the more stringent stand−by low power specifications. Just ground the Feed−back pin to force the NE1280 in shutdown mode.

NE1280 permanently monitors the output voltage, the coil current and the die temperature to protect the system from possible over−stresses.

NE1280 offers comprehensive protection coverage UVLO, Soft Start, Over−Power Limitation, Overvoltage protection, coil current limitation, Brown−Out Detection, Over−Power Limitation, thermal shutdown.

V_{DD} Undervoltage LockOut (UVLO)

The device incorporates an Undervoltage Lockout block to prevent the circuit from operating when V_{DD} is too low in order to ensure a proper operation. An UVLO comparator monitors V_{DD} pin voltage to allow the NE1280 to operate when V_{DD} exceeds 10.8V typically. The comparator incorporates some hysteresis (1.5V) to prevent erratic operation as the VDD crosses the threshold. When V_{DD} goes below the UVLO comparator lower threshold (9.3V typically), the circuit turns off. After startup, the operating range is between 9V and 28V.

Brown−Out Detection

NE1280 detects low AC line conditions and disables the PFC stage in this case. This protection mainly protects the power switch from the excessive stress that could damage it in such conditions.

Soft Start

VC is pulled low brown−out detection activates, or Undervoltage protection activates, and no drive is provided. At start up, the “200uA enhanced current source” is disabled. So there is only 32uA to charge the compensation components, and makes VC raise gradually. This is to obtain a slow increasing duty cycle and hence reduce the voltage and current stress on the MOSFET. Hence it provides a soft−start feature.

PRINCIPLE OF NE1280 OPERATION

CCM PFC Boost

A CCM PFC boost converter is shown in Figure 1. The input voltage is a rectified 50 ro 60Hz sinusoidal signal. The MOSFET is switching at a high frequency (typically 65kHz in NE1280) so that the inductor current I_L basically consists of high and low−frequency components.

Filter capacitor C_F is an essential and very small value capacitor in order to eliminate the high−frequency component of the inductor I_L. This filter capacitor cannot be too bulky because it can pollute the power factor by distorting the rectified sinusoidal input voltage.

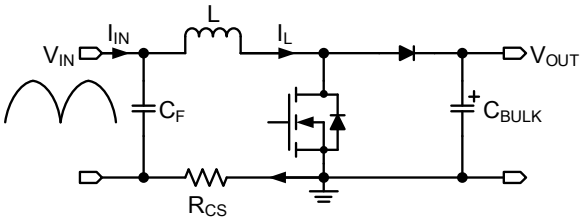


Figure 1 CCM PFC Boost Converter

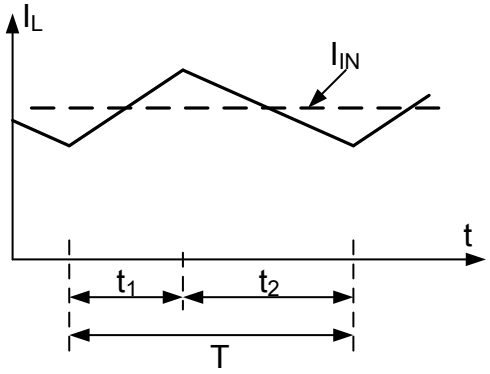


Figure 2 Inductor Current in CCM

PFC Methodology

The PFC methodology is described in this section.

As shown in Figure 2, the inductor current I_L in a switching period T includes a charging phase for duration t_1 and a discharging phase for duration t_2. The voltage conversion ratio is obtained in (Equation 1).

$$\frac{V_{OUT}}{V_{IN}} = \frac{t_1 + t_2}{t_2} = \frac{T}{T - t_1}$$

$$V_{IN} = \frac{T - t_1}{T} V_{OUT} \qquad \text{(Eq.1)}$$

where

V_{OUT} is the output voltage of PFC stage,

V_{IN} is the rectified input voltage,

T is the switching period,

t_1 is the MOSFET on time,

t_2 is the MOSFET off time.

The input filter capacitor C_F and the front−ended EMI filter absorbs the high−frequency component of inductor current I_L. It makes the input current I_{IN} a low−frequency signal only of the inductor current.

$$I_{IN} = I_{L-50} \qquad \text{(Eq.2)}$$

where

I_{IN} is the input AC current,

I_L is the inductor current.

I_{L-50} supposes a 50Hz operation. The suffix 50 means it is with a 50Hz bandwidth of the original I_L.

From (Equation 1) and (Equation 2), the input impedance Z_{IN} is formulated.

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{T - t_1}{T} \frac{V_{OUT}}{I_{L-50}} \qquad \text{(Eq.3)}$$

where Z_{IN} is input impedance.

Power factor is corrected when the input impedance Z_{IN} in (Equation 3) is constant or varies slowly in the 50 or 60Hz bandwidth.

The PFC modulation and timing diagram is shown in Figure 3. The MOSFET on time t_1 is generated by the intersection of reference voltage V_{REF} and ramp voltage V_{ramp}. A relationship in (Equation 4) is obtained.

$$V_{ramp} = V_M + \frac{I_{ch} t_1}{C_{ramp}} = V_{REF} \qquad \text{(Eq.4)}$$

V_{ramp} is the internal ramp voltage, the positive input of the PFC modulation comparator, V_M is the multiplier voltage appearing on V_M pin, I_{ch} is the internal charging current, C_{ramp} is the internal ramp capacitor, and V_{REF} is the internal reference voltage, the negative input of the PFC modulation comparator. I_{ch}, C_{ramp}, and V_{REF} also act as the ramp signal of switching frequency. Hence the charging current Ich is specially designed as in (Equation 5). The multiplier voltage V_M is therefore expressed in terms of t_1 in (Equation 6).

$$I_{ch} = \frac{C_{ramp} V_{REF}}{T} \quad \text{(Eq.5)}$$

$$V_M = V_{REF} - \frac{t_1}{C_{ramp}} \frac{C_{ramp} V_{REF}}{T} = V_{REF} \frac{T - t_1}{T} \quad \text{(Eq.6)}$$

From (Equation 3) and (Equation 6), the input impedance Z_{IN} is re−formulated in (Equation 7).

$$Z_{IN} = \frac{V_M}{V_{REF}} \frac{V_{OUT}}{I_{L-50}} \quad \text{(Eq.7)}$$

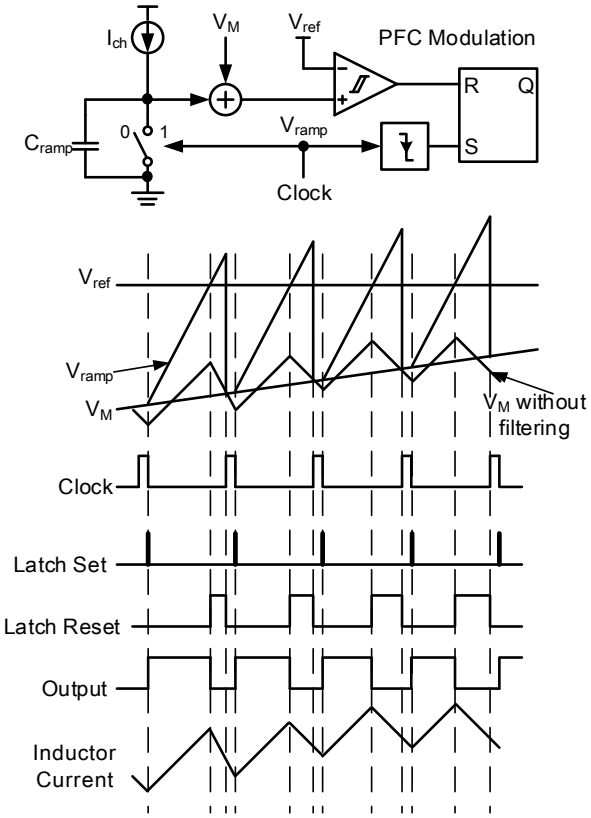


Figure 3 PFC Duty Modulation and Timeing Diagram

Because V_{REF} and V_{OUT} are roughly constant versus time, the multiplier voltage V_M is designed to be proportional to the I_{L-50} in order to have a constant Z_{IN} for PFC purpose.

It can be seen in the timing diagram in Figure 3 that V_M originally consists of a switching frequency ripple coming from the inductor current I_L. The duty ratio can be inaccurately generated due to this ripple. This modulation is the so−called “peak current mode”. Hence, an external capacitor C_M connected to the multiplier voltage V_M pin is essential to bypass the high−frequency component of V_M.The modulation becomes the so−called “average current mode” with a better accuracy for PFC.

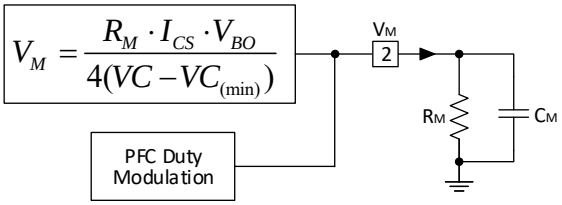


Figure 4 External Connection on V_M Pin

The multiplier voltage V_M is generated according to (Equation 8).

$$V_M = \frac{R_M \cdot I_{CS} \cdot V_{BO}}{4(VC - VC_{(\min)})} \qquad \text{(Eq.8)}$$

where

R_M is the external multiplier resistor connected to V_M pin, which is constant.

V_{BO} is the input voltage signal appearing on the BO pin, which is proportional to the rms input voltage.

I_{CS} is the sense current proportional to the inductor current.

I_L as described in (Equation 11).

VC is the control voltage signal, the output voltage of Operational Trans−conductance Amplifier (OTA), as described in (Equation 12).

R_M directly limits the maximum input power capability and hence its value affects the NE1280 to operate in either “follower boost mode” or “constant output voltage mode”.

Refer to Figure 5

$$V_{BO} = K_{BO}\widetilde{V_{IN}} = K_{BO} \cdot \frac{2\sqrt{2}}{\pi} V_{AC} \qquad \text{(Eq.9)}$$

$$K_{BO} = \frac{R_{BO\_DOWN}}{R_{BO\_UP} + R_{BO\_DOWN}} \qquad \text{(Eq.10)}$$

where

V_{BO} is the voltage on BO pin.

K_{BO} is the decay ratio of V_{IN} to V_{BO}.

$\widetilde{V}$ is the average voltage signal of V_{IN}, the voltage appearing on C_F.

R_{BO_DOWN} is low side resistor of the dividing resistors between V_{IN} and BO pin.

R_{BO_UP} is upper side resistor of the dividing resistors between V_{IN} and BO pin.

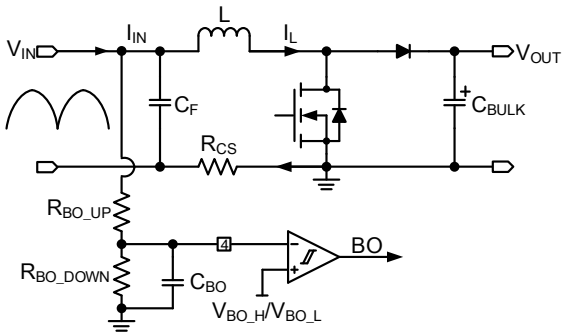


Figure 5 External Connection on BO Pin

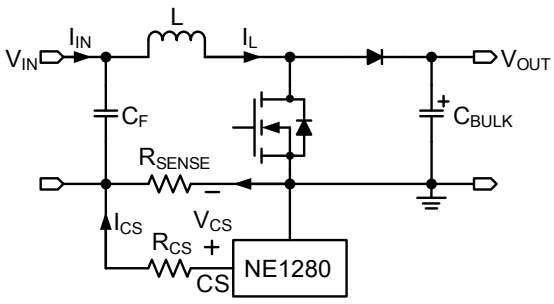


Figure 6 Current Sensing

Refer to Figure 6, sense current I_{CS} is proportional to the inductor current I_L as described in (Equation 11). I_L consists of the high−frequency component (that depends on di/dt or inductor L) and low−frequency component (that is I_{L-50}).

$$I_{CS} = \frac{R_{SENSE}}{R_{CS}} \cdot I_L \qquad \text{(Eq.11)}$$

where

R_{SENSE} is the sense resistor to sense I_L.

R_{CS} is the offset resistor between CS pin and R_{SENSE}.

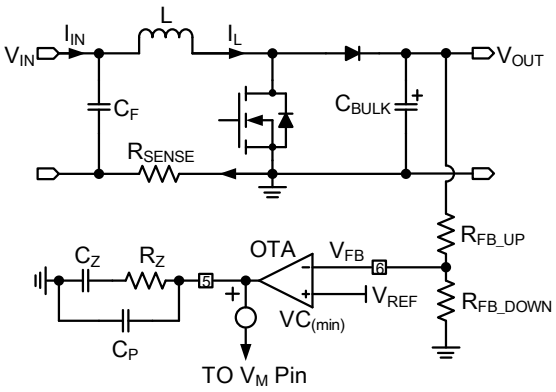


Figure 7 VC LPF

Refer to Figure 7, the Operational Trans−conductance Amplifier (OTA) senses V_{OUT} via the feedback resistor dividers, R_{FB_UP} and R_{FB_DOWN}. The OTA constructs a control voltage, VC, depending on the output power and hence V_{OUT}. The operating range of VC is from VC(min) to $VC_{(max)}$. The signal used for PFC duty modulation is after decreasing a offset voltage, $VC_{(min)}$, i.e. VC−$VC_{(min)}$.

This current I_C is a roughly constant current that comes from the PFC output voltage Vout that is a slowly varying signal. The bandwidth of I_C can be additionally limited by inserting the external type−2 compensation components (that are R_Z, C_Z, and C_P as shown in Figure 7). It is recommended to limit fc, that is the bandwidth of VC (or I_C), below 20 Hz typically to achieve power factor correction purpose.

The transformer of V_{OUT} to VC is as described in (Equation 12) if C_Z is >> C_P. G_{EA} is the error amplifier gain.

$$\frac{VC}{V_{OUT}} = \frac{R_{FB\_DOWN} \cdot G_{EA} \cdot R_Z}{R_{FB\_DOWN} + R_{FB\_UP}} \cdot \frac{1 + sR_ZC_Z}{sR_ZC_Z(1 + sR_ZC_P)} \qquad \text{(Eq.12)}$$

From (Equation 7) − (Equation 11), the input Impedance Z_{IN} is re−formulated in (Equation 13).

$$Z_{IN} = \frac{\sqrt{2}R_M R_{SENSE} V_{OUT} V_{AC} K_{BO} I_L}{2\pi R_{CS} \cdot (VC - VC_{(\min)}) \cdot V_{REF} \cdot I_{L-50}} \qquad \text{(Eq.13)}$$

When I_L is equal to I_{L-50}, (Equation 13) is re−formulated in (Equation 14).

$$Z_{IN} = \frac{\sqrt{2}R_M R_{SENSE} V_{OUT} V_{AC} K_{BO}}{2\pi R_{CS} \cdot (VC - VC_{(\min)}) \cdot V_{REF}} \qquad \text{(Eq.14)}$$

The multiplier capacitor C_M is the one to filter the high−frequency component of the multiplier voltage V_M. The high −frequency component is basically coming from the inductor current I_L. On the other hand, the filter capacitor C_F similarly removes the high−frequency component of inductor current I_L. If the capacitors C_M and C_F match with each other in terms of filtering capability, I_L becomes I_{L-50}. Input impedance Z_{IN} is roughly constant over the bandwidth of 50 or 60Hz and power factor is corrected.

Input and output power (P_{IN} and P_{OUT}) are derived in (Equation 15) when the circuit efficiency η is obtained or assumed. The variable V_{AC} stands for the rms input voltage.

$$P_{IN} = \frac{V_{AC}^{\ 2}}{Z_{IN}} = \frac{2\pi R_{CS}(VC - VC_{(\min)})V_{REF}V_{AC}}{\sqrt{2}R_M R_{SENSE}V_{OUT}K_{BO}} \propto \frac{(VC - VC_{(\min)})V_{AC}}{V_{OUT}} \quad \text{(Eq.15)}$$

$$P_{OUT} = \eta P_{IN} = \eta \frac{2\pi R_{CS}(VC - VC_{(\min)})V_{REF}V_{AC}}{\sqrt{2}R_M R_{SENSE}V_{OUT}K_{BO}} \propto \frac{(VC - VC_{(\min)})V_{AC}}{V_{OUT}} \quad \text{(Eq.16)}$$

Follower Boost

The “Follower Boost” is an operation mode where the pre−converter output voltage stabilizes at a level that varies linearly versus the ac line amplitude. This technique aims at reducing the gap between the output and input voltages to optimize the boost efficiency and minimize the cost of the PFC stage.

NE1280 operates in follower boost mode when VC is constant, i.e. VC raises to its maximum value $VC_{(max)}$. Re −formulate (Equation 16) to become(Equation 17) and (Equation 18) by replace VC by $VC_{(max)}$. If VC is constant based on (Equation 15), for a constant load or power demand the output voltage V_{OUT} of the converter is proportional to the rms input voltage V_{AC}. It means the output voltage V_{OUT} becomes lower when the rms input voltage V_{AC} becomes lower. On the other hand, the output voltage V_{OUT} becomes lower when the load or power demand becomes higher.

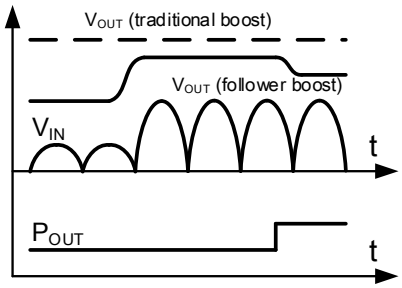


Figure 8 Follower Boost Characteristics

$$P_{OUT} = \eta \frac{2\pi R_{CS}(VC_{(\max)} - VC_{(\min)})V_{REF}V_{AC}}{\sqrt{2}R_M R_{SENSE}V_{OUT}K_{BO}} = \eta \frac{2\pi R_{CS} \cdot \Delta VC \cdot V_{REF} \cdot V_{AC}}{\sqrt{2}R_M R_{SENSE}V_{OUT}K_{BO}} \quad \text{(Eq.17)}$$

$$V_{OUT} = \eta \frac{2\pi R_{CS}\Delta VC \cdot V_{REF}}{\sqrt{2}R_M R_{SENSE}K_{BO}} \cdot \frac{V_{AC}}{P_{OUT}} \quad \text{(Eq.18)}$$

where

$VC_{(max)}$ is the maximum control voltage.

ΔVC is the gap between $VC_{(max)}$ and $VC_{(min)}$.

It is illustrated in Figure 8.

Follower Boost Benefits

The follower boost circuit offers and opportunity to reduce the output voltage Vout whenever the rms input voltage V_{AC} is lower or the power demand P_{OUT} is higher. Because of the step−up characteristics of boost converter, the output voltage V_{OUT} will always be higher than the input voltage V_{IN} even though V_{OUT} is reduced in follower boost operation. As a result, the on time t1 is reduced. Reduction of on time makes the loss of the inductor and power MOSFET smaller. Hence, it allows cheaper cost in the inductor and power MOSFET or allows the circuit components to operate at a lower stress condition in most of the time.

Output Feedback

The output voltage Vout of the PFC circuits is sensed at V_{FB} pin via the resistor divider (R_{FB_DOWN} and R_{FB_UP}) as shown in Figure7. Vout is regulated as described in (Equation 19).

$$V_{OUT} = V_{REF} \cdot \frac{R_{FB\_UP} + R_{FB\_DOWN}}{R_{FB\_DOWN}} \qquad \text{(Eq.19)}$$

The feedback signal V_{FB} represents the output voltage V_{OUT} and will be used in the output voltage regulation, Overvoltage protection (OVP), fast transient response, and Undervoltage protection (UVP).

Current Sense

The device senses the inductor current I_L by the current sense scheme in Figure6. The device maintains the voltage at CS pin to be zero voltage (i.e., Vcs ≈ 0V) so that (Equation 11)

$$I_{CS} = \frac{R_{SENSE}}{R_{CS}} I_L$$

can be formulated.

This scheme has the advantage of the minimum number of components for current sensing. The sense current I_{CS} represents the inductor current I_L and will be used in the PFC duty modulation to generate the multiplier voltage V_M, Over−Power Limitation (OPL), and Over−Current Protection. (Equation 11) would insist in the fact that it provides the flexibility in the R_{SENSE} choice and that it allows to detect in−rush currents.

Over−Current Protection (OCP)

Over−Current Protection is reached when I_{CS} is larger than $I_{S(OCP)}$ (200uA typical). The offset voltage of the CS pin is typical 10mV and it is neglected in the calculation. Hence, the maximum OCP inductor current threshold $I_{L(OCP)}$ is obtained in (Equation 20).

$$I_{L(OCP)} = \frac{R_{CS} I_{S(OCP)}}{R_{SENSE}} = \frac{R_{CS}}{R_{SENSE}} \cdot 200\mu A \qquad \text{(Eq.20)}$$

When over−current protection threshold is reached, the Drive Output of the device goes low. The device automatically resumes operation when the inductor current goes below the threshold.

Input Voltage Sense

The device senses the rms input voltage V_{AC} by the sensing scheme in Figure14. V_{BO} senses the average rectified input voltage V_{IN} via the resistor divider. An external capacitor C_{BO} is to maintain the V_{BO} the average value of V_{IN}. V_{BO} is used for Brown−Out Protection, PFC duty modulation and over−power limitation (OPL).

Brown−Out Protection

NE1280 uses the V_{BO} signal to protect the PFC stage from operating as the input voltage is lower than expected. Re−formulate (Equation 9) to get (Equation 21). Before the device operates, V_{IN} is equal to the peak value of rms input voltage, V_{AC}. Hence V_{BO} is as described in (Equation 21).

$$V_{BO} = \frac{R_{BO\_DOWN}}{R_{BO\_DOWN} + R_{BO\_UP}} \widetilde{V_{IN}} = \frac{R_{BO\_DOWN}}{R_{BO\_DOWN} + R_{BO\_UP}} \cdot \sqrt{2} V_{AC} \qquad \text{(Eq.21)}$$

After device operates, V_{IN} is the rectified sinusoidal input voltage. Thanks to C_{BO}, V_{BO} is the average of rectified input voltage. Hence V_{BO} decays to 2/π of the peak value of rms input voltage V_{AC} as described in (Equation 22).

$$V_{BO} = \frac{R_{BO\_DOWN}}{R_{BO\_DOWN} + R_{BO\_UP}} \frac{2\sqrt{2}}{\pi} V_{AC} \qquad \text{(Eq.22)}$$

Hence a larger hysteresis of the brown out comparator is needed, which is 0.7V typical in this device. When V_{BO} goes below than V_{BOL} (0.7V typical), the device turns off the Drive output and keeps it off till V_{BO} exceeds V_{BOH} (1.3V typical). When the device awakes after an off−state (Undervoltage lockout or shutdown), the default threshold is V_{BOH}.

Overpower Limitation (OPL)

This is a second OCP with a threshold that is line dependent. Sense current I_{CS} represents the inductor current I_L and hence represents the input current approximately. Input voltage signal V_{BO} represents the rms input voltage. The product ($I_{CS} \times V_{BO}$) represents an approximated input power ($I_L \times V_{AC}$). It is illustrated in Figure 9.

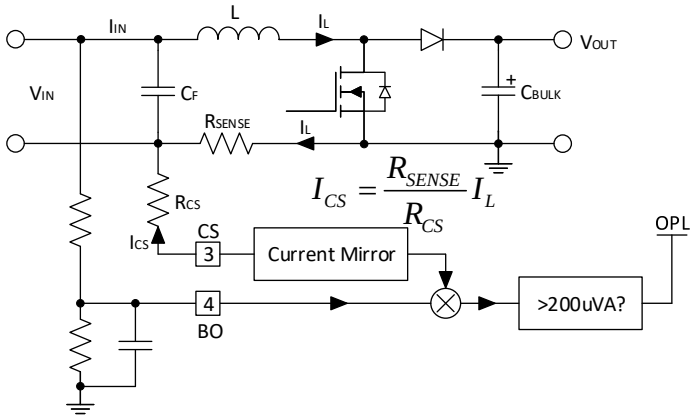


Figure 15 Over-Power Limitation

When the product (ICS×VBO) is greater than a permissible level 200uVA, the device turns off the drive output so that the input power is limited. The OPL is automatically deactivated when the product (ICS×VBO) is lower than the 200uVA level. This 200 uVA level corresponds to the approximated input power (IL ×VAC) to be smaller than the particular expression in (Equation 23).

$$I_{CS} \times V_{BO} < 200\mu VA \qquad \text{(Eq.23)}$$

$$(I_L \frac{R_{SENSE}}{R_{CS}}) \cdot (\frac{2\sqrt{2}K_{BO}}{\pi} \cdot V_{AC}) < 200\mu VA$$

$$I_L \cdot V_{AC} < \frac{R_{CS} \cdot \pi}{R_{SENSE} \cdot K_{BO}} \cdot 50\sqrt{2}\mu VA$$

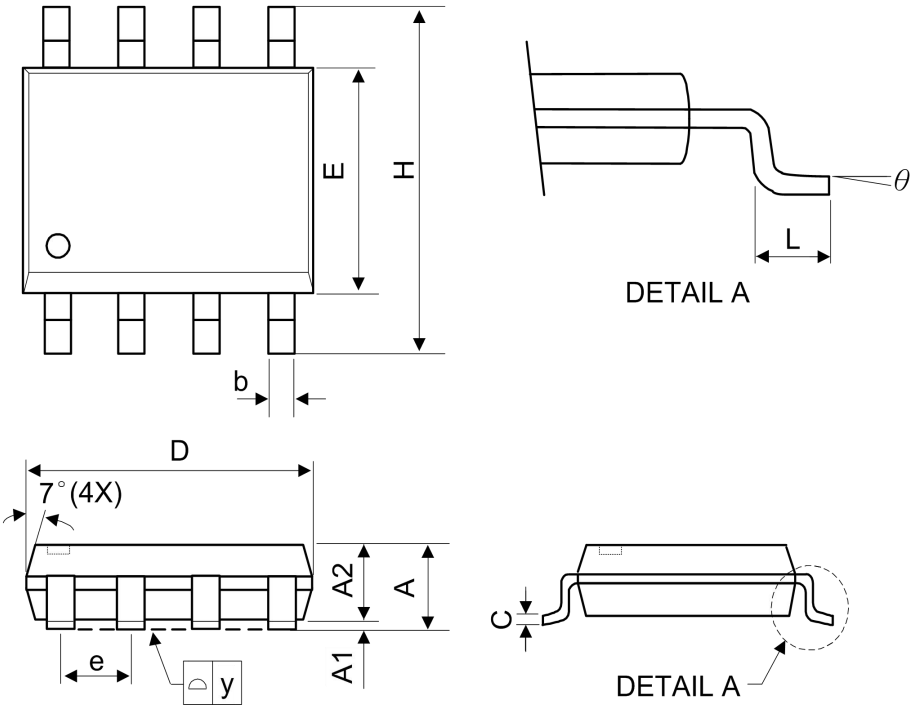
Undervoltage Protection (UVP) for Open Loop Protection or Shutdown

When V_{FB} is less than 8% of V_{REF}, NE1280 is shut down and consumes less than 500uA. The device automatically starts operation when the output voltage goes above 12% of V_{REF}. In normal situation of boost converter configuration, the output voltage V_{OUT} is always greater than the input voltage Vin and the feedback signal V_{FB} is always greater than 8% and 12% of V_{REF} to enable NE1280 to operate.

The Undervoltage Protection function can reach open loop protection, such as V_{FB} is shorted to ground or the feedback resistor R_{FB_UP} is open. It also can disables the PFC stage and forces a low consumption mode. This feature helps to meet stringent stand−by specifications. Power Factor being not necessary in stand−by, the PFC stage is generally inhibited to save the pre−converter losses. To further improve the stand−by performance, the PFC controller should consume minimum current in this mode.

Package Information

SOP-8



Symbol	Millimetre			Inch		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.75	-	-	0.069
A1	0.1	-	0.25	0.04	-	0.1
A2	1.25	-	-	0.049	-	-
C	0.1	0.2	0.25	0.0075	0.008	0.01
D	4.7	4.9	5.1	0.185	0.193	0.2
E	3.7	3.9	4.1	0.146	0.154	0.161
H	5.8	6	6.2	0.228	0.236	0.244
L	0.4	-	1.27	0.015	-	0.05
b	0.31	0.41	0.51	0.012	0.016	0.02
e	1.27 BSC			0.050 BSC		
y	-	-	0.1	-	-	0.004
θ	0°	-	8°	0°	-	8°