

Description

The NE1289 is a dual-channel synchronous rectifier (SR) controller for high performance power system. With the ultra-low quiescent current, appropriate gate drive method and independent sampling input, the NE1289 can achieve maximum efficiency under different load conditions. The NE1289 operates over a wide supply voltage range from 4.6V to 36V, which is suitable for a variety of application scenarios. With dual-channel drivers and independent differential sampling, it is easy to use. The extremely low turn-off propagation delay time (10ns) and high sink current ($\sim 2.5A$) capability of the driver reduce SR MOSFET VDS stress. The unique VG clamping circuit prevents VG from turning on by fast rising at VD pin under low VCC condition, that avoids the shoot through between primary side and secondary side during system startup.

The NE1289 has appropriate logical protection features, two-channel interlock logic with proper interlock time to make the system more reliable.

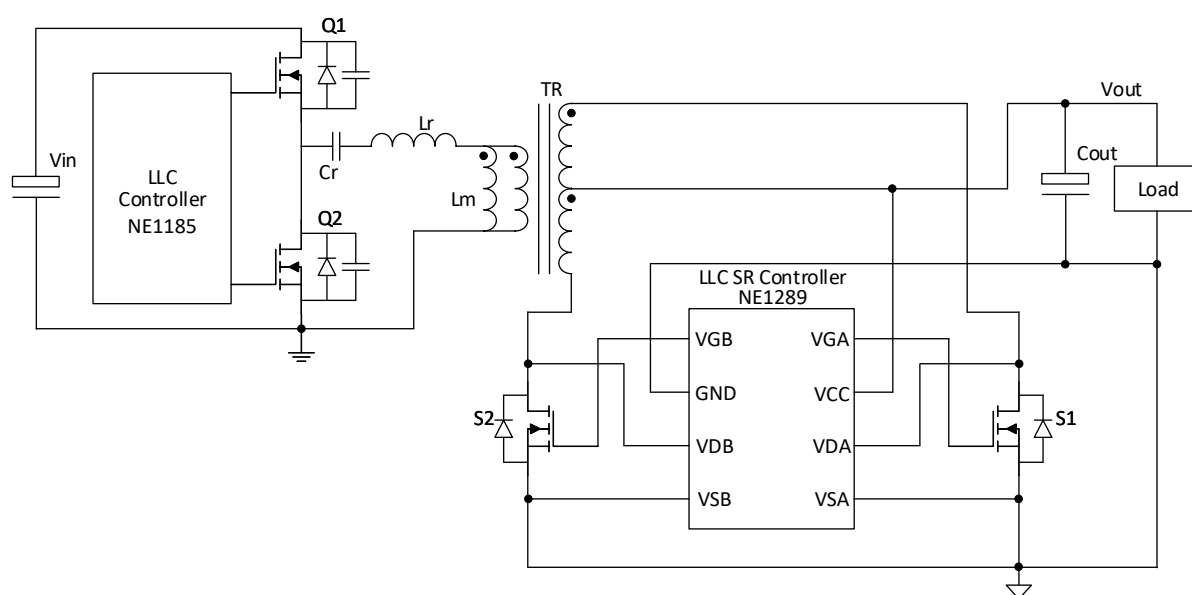
Features

- Wide VCC Voltage Range from 4.6V-36V
- Ultra-Low Quiescent Current $<100\mu A$
- Reduces the Chance of False Triggering in Discontinuous Conduction Mode (DCM)
- 10ns Fast Turn-off Delay
- VGA/VGB Clamping Circuit for Low V_{th} SR MOSFET
- -3V Drain Voltage Spike Tolerance
- True Differential Inputs for VDS Sensing of Each SR MOSFET
- Interlock Logic Between Two-Channel
- Adaptive Gate Drive for Maximum Efficiency
- Available in SOP-8 Package

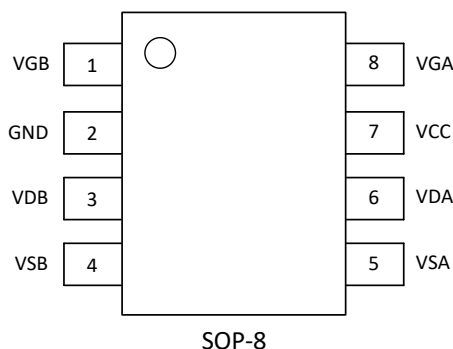
Applications

- AC/DC Adapters for Mobile Phone and Notebook
- Industrial Power Supplies
- Desktop All-in-one PC Power Supplies
- High Power Density Power Supplies

Typical Application



Pin Configuration



Functional Pin Description

Pin No.	Name	Description
1	VGB	B channel MOSFET gate drive output.
2	GND	Analog ground.
3	VDB	B channel MOSFET drain sense input.
4	VSB	B channel MOSFET source sense input.
5	VSA	A channel MOSFET source sense input.
6	VDA	A channel MOSFET drain sense input.
7	VCC	Supply voltage.
8	VGA	A channel MOSFET gate drive output.

Ordering Information

Product model	Packaging form	Smallest packaging	Logo
NE1289	SOP-8	4000PCS	NE1289

Absolute Maximum Ratings ⁽¹⁾

Symbol	Parameter	MIN	MAX	Units
VCC	supply voltage VCC	-0.3	38	V
VGA/VGB ⁽²⁾	voltage on pin VGA and VGB	-0.3	14	
VDA/VDB	drain sense voltage VDA and VDB	-1	105	
VDA/VDB ⁽³⁾	drain sense voltage VDA and VDB	-3	115	
VSA/VSB	source sense voltage VSA and VSB	-0.4	0.4	
T _J	operating junction temperature,	-40	150	°C
T _{stg}	storage temperature	-55	150	
T _{sld}	soldering temperature (10 second)		260	

(1) Stresses beyond the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in "RECOMMENDED OPERATING CONDITIONS". Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Output pin not to be voltage driven.

(3) Repetitive Pulse < 200ns.

ESD Ratings

		Value	Units
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±2000	V

Notes:

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

		MIN	MAX	Units
Recommended Operation Conditions	VCC supply voltage	4.6	36	V
	drain sense voltage VDA and VDB	-0.7	100	
	operating junction temperature. (T _J)	-40	125	°C

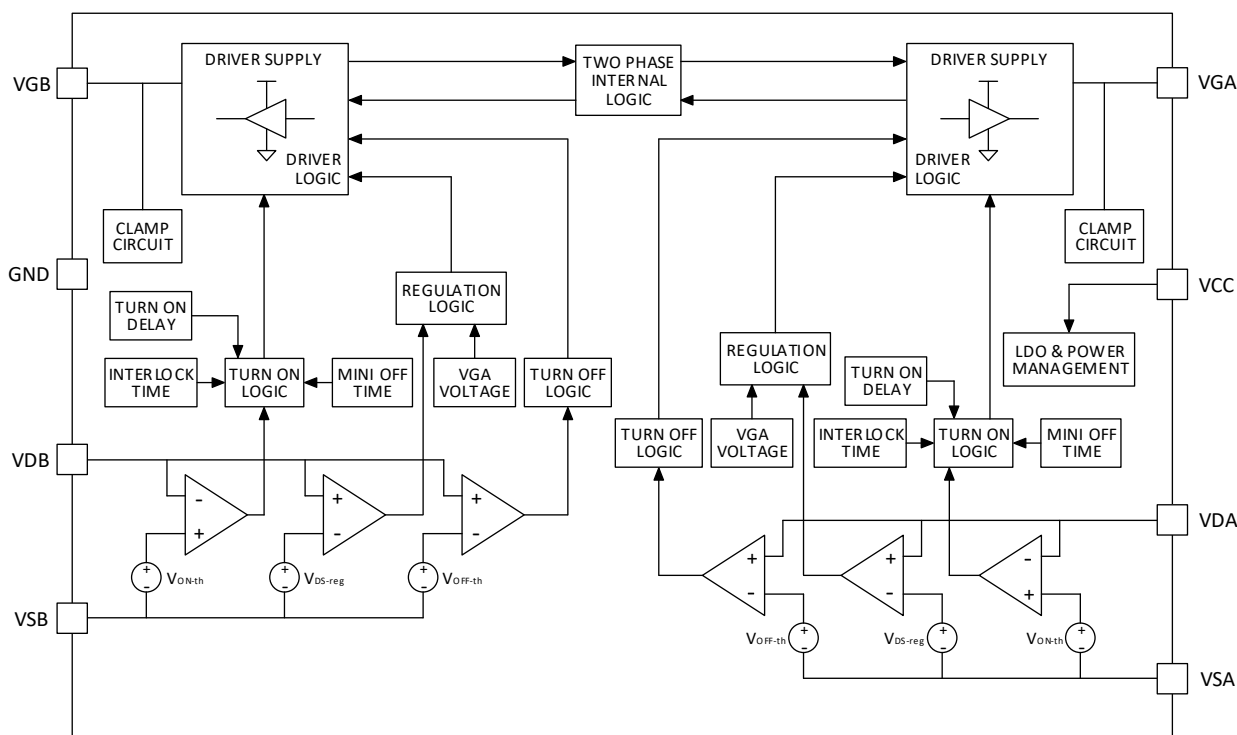
Thermal Information

		Value	Units
Package Thermal Resistance ⁽¹⁾	θ_{JA} (Junction to ambient)	90	°C/W
	θ_{JC} (Junction to case)	45	

Note:

- (1) Measured on JESD51-7, 4-layer PCB.

Electrical Characteristics



Electrical Characteristics

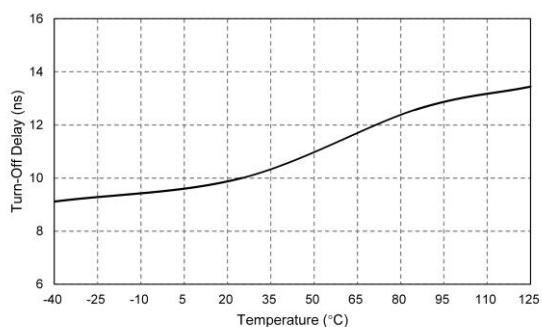
$T_A=25^{\circ}\text{C}$. All Voltages are measured with respect to ground (pin 2). Currents are positive when flowing into the IC, unless otherwise specified.

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
Supply voltage Management						
V_{CC-ON}	VCC UVLO rising		4.25	4.40	4.55	V
V_{CC-OFF}	VCC UVLO falling		4.05	4.20	4.35	V
$V_{CC-HYST}$	VCC UVLO hysteresis			0.2		V
I_{CC}	Operating supply current	VCC=12V, VDA=VDB=10V		75	100	μA
		VCC=12V VDA=VDB=0V		0.85	1.05	mA
t_{act}	Sleep-mode activation time		80	110	160	μs
Synchronous rectification sense input						
V_{DS-reg}	$V_{DA(B)} - V_{SA(B)}$ Adjusting voltage	VCC=8V	-45	-25		mV
V_{ON-th}	$V_{DA(B)} - V_{SA(B)}$ Turn-on threshold voltage	VCC=12V	-450	-300	-150	mV
V_{OFF-th}	$V_{DA(B)} - V_{SA(B)}$ Turn-off threshold voltage	VCC=13V	110	150	190	mV
T_{D-on}	Turn-on propagation delay time	$C_{LOAD} = 0\text{nF}$, VD step down from 3V to -0.3V, measure VG rising to 1V	50	60	75	ns
T_{D-off}	Turn-off propagation delay time	$C_{LOAD} = 0\text{nF}$, VD step up from -0.3V to 3V, measure VG falling to 90% of V_{G-H}	5	10	15	ns
T_{B-on}	Turn-on blanking time ⁽¹⁾	$C_{LOAD} = 0\text{nF}$, VCC=12V		0.8		μs
T_{B-off}	Turn-off blanking time	$C_{LOAD} = 0\text{nF}$, VCC=12V	0.7	0.8		μs
T_d	Two-channel interlock time	$C_{LOAD} = 0\text{nF}$, VCC=12V	50	65	80	ns
V_{B-off}	$V_{DA(B)} - V_{SA(B)}$ Turn-off threshold during turn-on blanking time ⁽¹⁾			0.5		V
Gate Driver						
V_{G-H} (high)	Maximum gate voltage	VGA/VGB at VCC=5V	4.85	4.99	5	V
		VGA/VGB at VCC=12V	9.5	10.5	11.5	V
		VGA/VGB at VCC=24V	9.5	10.5	11.5	V
I_{VG-H}	Maximum source current ⁽¹⁾			-0.25		A
I_{VG-L}	Maximum sink current ⁽¹⁾			2.5		A
R_{sink}	Pull-down impedance ⁽¹⁾	$I_{LOAD} = 100\text{mA}$		0.9		Ω

Note:

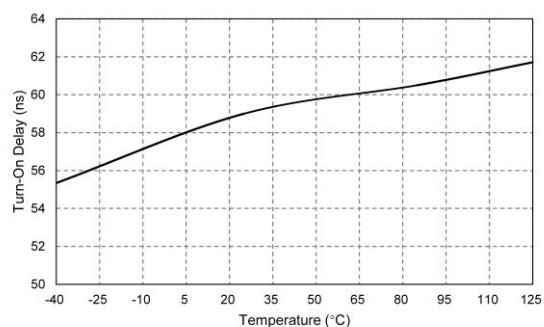
(1) Values are verified by characterization on bench, not tested in production.

Typical Characteristics



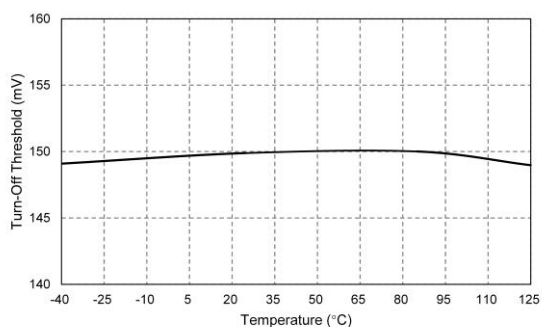
VCC=12V, C_{LOAD}=0nF

Turn-Off Delay vs Temperature



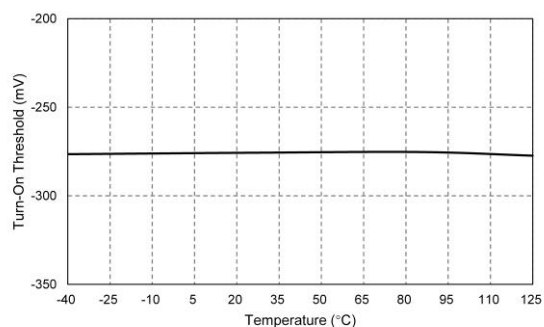
VCC=12V, C_{LOAD}=0nF

Turn-On Delay vs Temperature



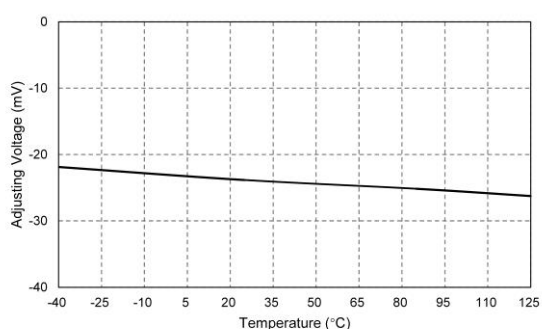
VCC=12V, C_{LOAD}=0nF

Turn-Off Threshold vs Temperature

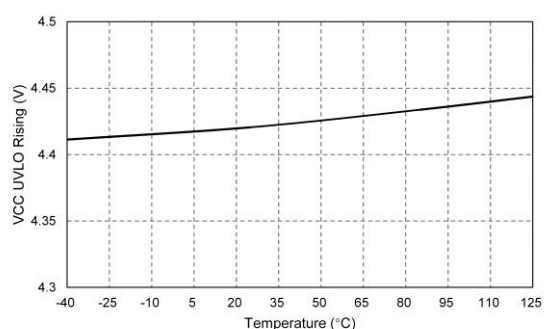


VCC=12V, C_{LOAD}=0nF

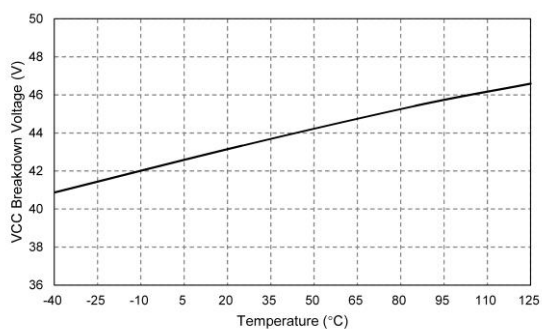
Turn-On Threshold vs Temperature



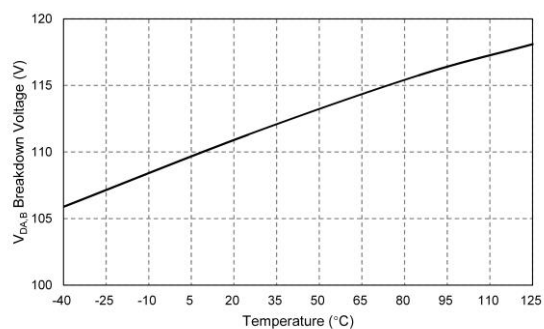
Adjusting Voltage vs Temperature



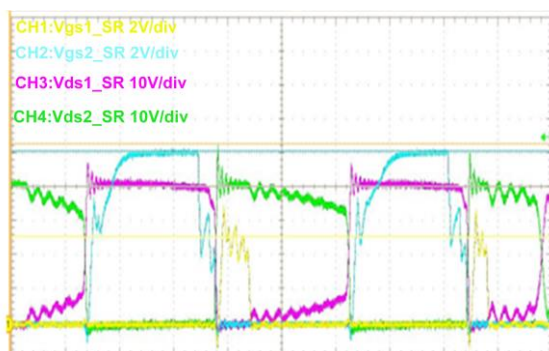
VCC UVLO Rising vs Temperature



VCC Breakdown Voltage vs Temperature

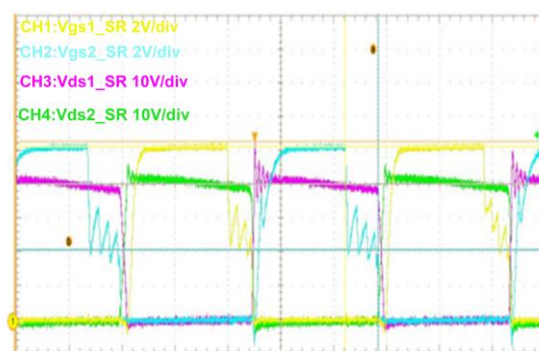


VDA/B Breakdown Voltage vs Temperature



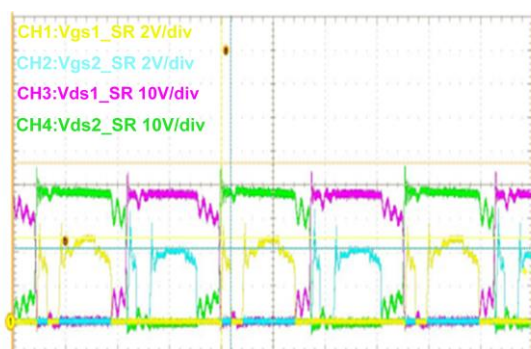
$V_{in}=230VAC$, $V_{out}=20V$, $I_{out}=0.1A$

Operation in 300W LLC Converter



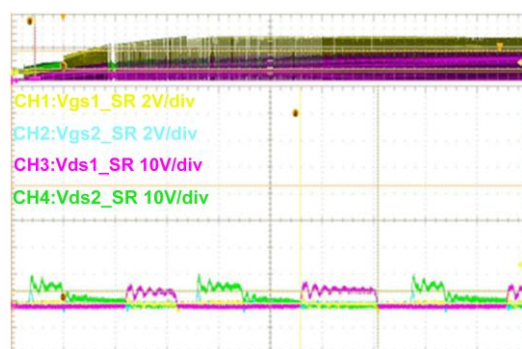
$V_{in}=230VAC$, $V_{out}=20V$, $I_{out}=15A$

Operation in 300W LLC Converter



$V_{in}=230VAC$, $V_{out}=20V$, $I_{out}=1A$ Turn-Off

Operation in 300W LLC Converter



$V_{in}=230VAC$, $V_{out}=20V$, $I_{out}=0.1A$ Turn-On

Operation in 300W LLC Converter

Detailed Description

Overview

The NE1289 is a dual-channel synchronous rectifier controller capable of driving two N-Channel power MOSFETs in resonant converter applications. This controller has dual differential sampling inputs to detect the voltage difference between the drain and source of each SR MOSFET.

The gate voltage is adjusted consistently with the VDS voltage. The control strategy of the chip is easy to implement and straight-forward.

The unique VG clamping circuit works well to prevent VG from turning on by quickly rising at the VD pin with no VCC. Extremely low turn-off propagation delay time (10ns) and high sink current (~2.5A) capability of the driver reduce SR MOSFET VDS stress. Internal two-channel interlock logic with proper interlock time makes the system more reliable.

VCC Power Supply and Undervoltage Lockout

The NE1289 operates from a supply voltage of 4.6V to 36V. This feature makes NE1289 suitable for a variety of application scenarios. For the best performance, Use a typical 0.1uF decoupling capacitor as close as possible between the VCC and GND pins of NE1289. A VCC bypass capacitor (1uF to 10uF) in parallel to the decoupling capacitor is also recommended to reduce noise ripple during switching.

NE1289 has an internal undervoltage lockout (UVLO) protection feature in the VCC supply circuit blocks. When the voltage on the VCC pin exceeds V_{CC-ON} , the controller leaves the UVLO state and activates the SR circuitry. When VCC voltage drops to below V_{CC-OFF} , the controller re-enters the UVLO state.

Conduction Phase

When the absolute voltage difference of VDS is greater than V_{ON-th} , the corresponding gate driver output turns on the external SR MOSFET.

After SR MOSFET turns on, a turn-on blanking time T_{B-on} is required to prevent the parasitic ringing from falsely turning off SR MOSFET. During the turn-on blanking time, the turn-off threshold increases to V_{B-off} .

After this, the NE1289 goes into regulation mode. In this phase, NE1289 adjusts the VDS of SR MOSFET to be around V_{DS-reg} until the current through SR MOSFET drops to zero.

Turn-Off Phase

After the turn-on blanking time T_{B-on} , the turn-off threshold is around V_{OFF-th} . With a suitable regulation and turn-off strategy, the NE1289 will not turn-off prematurely, which will not cause the current to conduct for a long time through the body diode of the SR MOSFET.

With an extremely fast 10ns turn-off propagation delay and 2.5A pull-down (sink) current, the NE1289 is rapidly turned off when the current through the external SR MOSFET reaches zero. After SR MOSFET turns off, a minimum turn-off blanking time T_{B-off} is required, which helps to reduce the chance of false triggering in DCM.

Interlock Function

The NE1289 incorporates an internal interlock logic between the two drivers, which prevents the SR MOSFETs from cross conduction.

The control diagram is shown on Figure 1. When either VGA or VGB is turned on, the other channel gate driver is blanked until channel VGA or VGB is turned off.

After either VGA or VGB is unlocked, the other channel gate driver has to lock until the end of the interlock time (T_d).

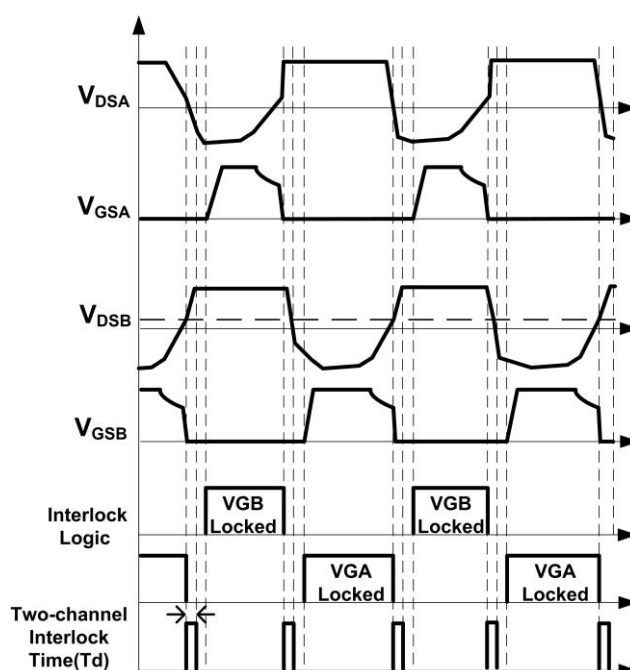


Figure 1. Internal Interlock Logic Control Diagram

Application and Implementation

Typical Applications

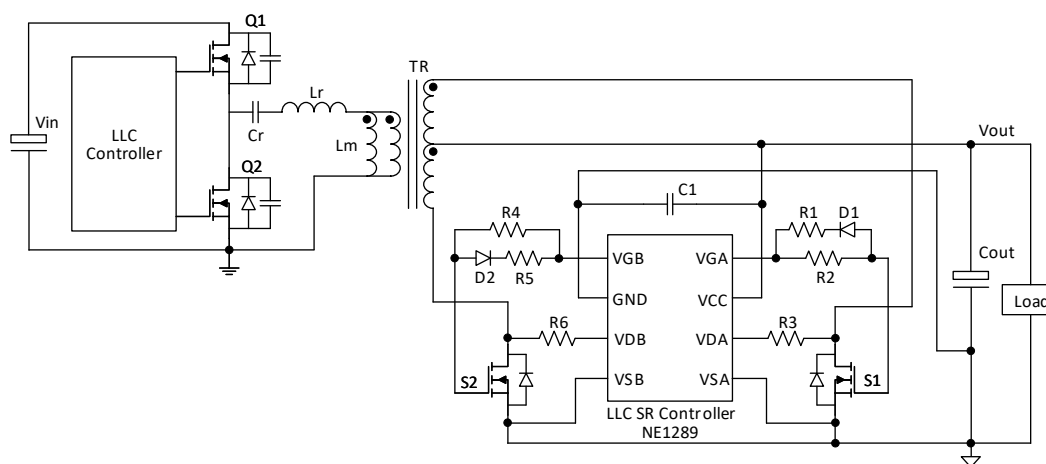


Figure 2. NE1289 Reference Design Circuit

Design Procedure

Supply Voltage

The supply voltage applied to the controller VCC pin should never exceed the absolute maximum ratings. Higher supply voltages require consideration of chip power dissipation and junction temperature (See Section *Power Dissipation*). In some scenarios where the output bus voltage is high (for example, applications with outputs greater than 36V), a high voltage LDO must be used so that the VCC pin does not exceed the absolute maximum ratings and reduces the power dissipation of the internal LDO.

NE1289 reference design circuit is shown in Figure 2, Connect a low-ESR ceramic decoupling capacitor (C1) between 100 nF and 1 μ F from VCC to GND for stability. The choice of decoupling capacitor voltage rating should also depend on the VCC voltage. Place the capacitor (C1) as close as possible to the NE1289 VCC and GND pins.

Peak Source and Sink Current

In order to reduce the switching losses and stress of the MOSFET, the switching speed of the MOSFET during turn-on and turn-off should be considered. The chip should be able to provide the required peak current for achieving the targeted switching speeds with the targeted power MOSFET. The maximum source and sink currents of the NE1289 have been provided.

For system applications, adding resistors R2 and R4 (such as 1 Ω or 2 Ω) between the gate of MOSFET and the V_{GA}/V_{GB} controls the switching speed of the MOSFET. Add diodes D1 and D2 as well as resistors R1 and R5. Keep the Values of the resistors at 0 Ω to achieve the fastest turn-off time.

Adjusting Voltage Setup

During regulation mode, NE1289 adjusts the V_{DS} of SR MOSFET to be around V_{DS-reg} until the current through the SR MOSFET drops to zero.

In different application systems, V_{DS-reg} is one of the important parameters, which determines the output level of the gate driver. When the current of the MOSFET rises to a higher value, the V_{DS} voltage is less than the V_{DS-reg} voltage. The gate driver charges the gate of the MOSFET until the MOSFET is fully turned on. Therefore, the value of V_{DS-reg} is related to system efficiency.

If really needed, the value of V_{DS-reg} may be slightly fine-tuned by adding resistors R3 and R6 (R_{set}) between the drain of the MOSFET and V_{DA}/V_{DB}. It is approximately calculated based on the below formula. The default value of R3 and R6 is zero ohm.

$$V_{DS_regnew} \approx V_{DS_reg} - (40\mu A \times R_{set})$$

Power Dissipation

The chip power consumption and junction temperature must be considered. The chip will be damaged, if these two parameters are too large. The total power consumption (P_{DIS}) is estimated by the following formula:

$$P_{DIS} = P_{DRV} + P_P$$

The gate power (P_{DRV}) needs to be calculated first. It is calculated based on the formula:

$$P_{DRV} = 2 \times (Q_g - Q_{gd}) \times f_{smax} \times V_{CC}$$

Where (Q_g-Q_{gd}) is the total gate charge for SR MOSFET, f_{smax} is the maximum switching frequency, and V_{CC} is the supply voltage. The power consumption P_p (without gate charge) must also be considered.

$$P_P = I_{CC} \times V_{CC}$$

I_{CC} is the normal operating supply current without gate charging. The operating junction temperature (T_{JOP}) at a given ambient temperature (T_A) can be estimated according to the formula:

$$T_{JOP} = \theta_{JA} \times P_{DIS} + T_A$$

θ_{JA} is the junction-to-ambient thermal resistance.

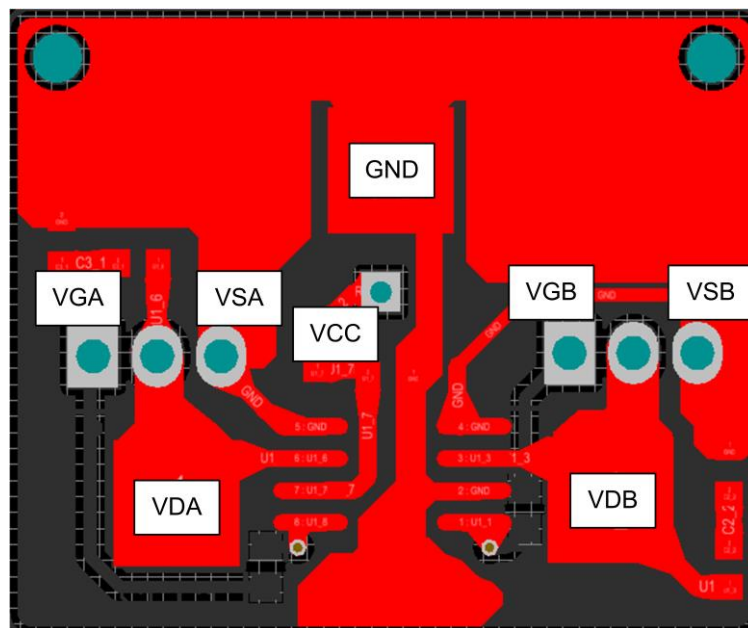
Layout

Layout Guidelines

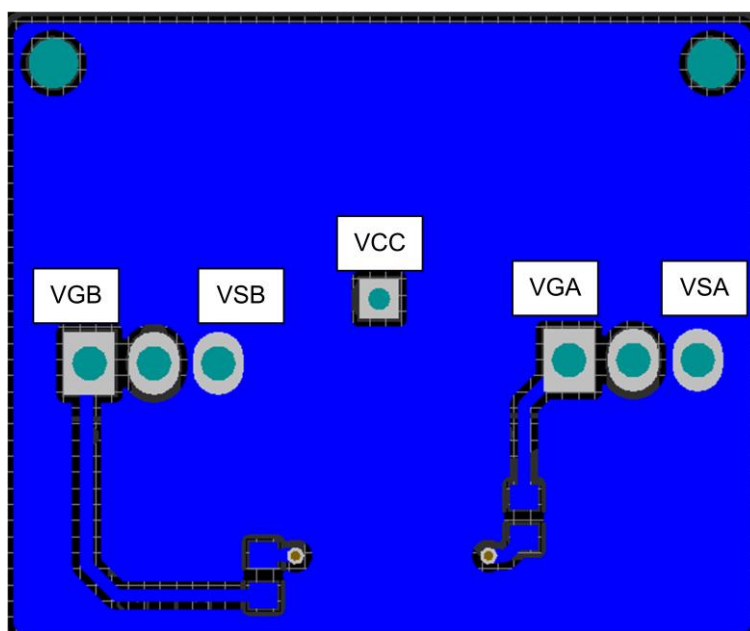
To achieve high performance of the NE1289, the following layout tips must be followed.

1. Use separate clean traces for VCC and GND pins.
2. At least one low-ESR ceramic bypass capacitor(100nF) must be used. Place the capacitor as close as possible to the NE1289 VCC and GND pins.
3. The GND pin on the ground plane needs to route with a short and wide trace, or use a GND plane underneath the IC connected to the GND pin as well. It results in better heat dissipation.
4. Use separate traces for each source sense pin (VSA/VSB), and keep the ground and source sense traces separated.
5. Keep the two-channel differential sampling inputs (VDA/VSA, VDB/VSB) to each of the corresponding MOSFET drain/source pins as short as possible.
6. Keep the loop area of the two-channel differential sampling inputs (VDA/VSA, VDB/VSB) to each corresponding MOSFET drain/source pins as small as possible.
7. Avoid placing the VDA, VSA, VDB, and VSB traces close to any other high dV/dT traces that would induce significant noise into the high impedance leads.
8. The trace from the VGA/VGB pin to the gate of the SR MOSFET needs to be as short as possible.

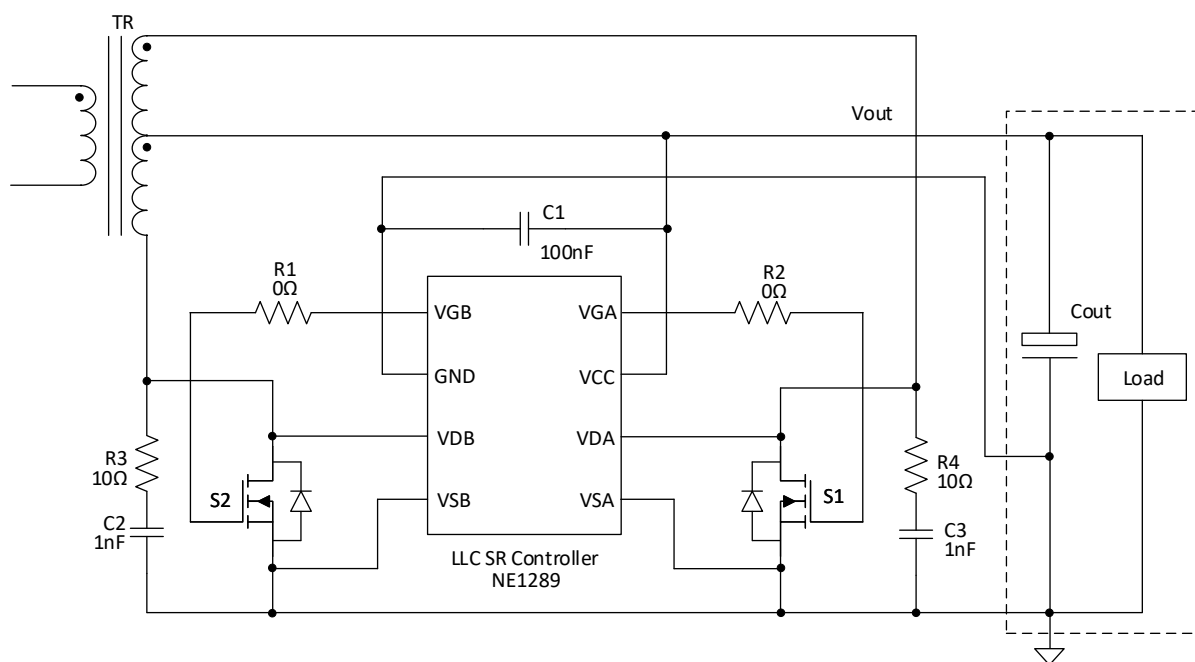
Layout Example



NE1289 Demo Board Layout (Top Layer)



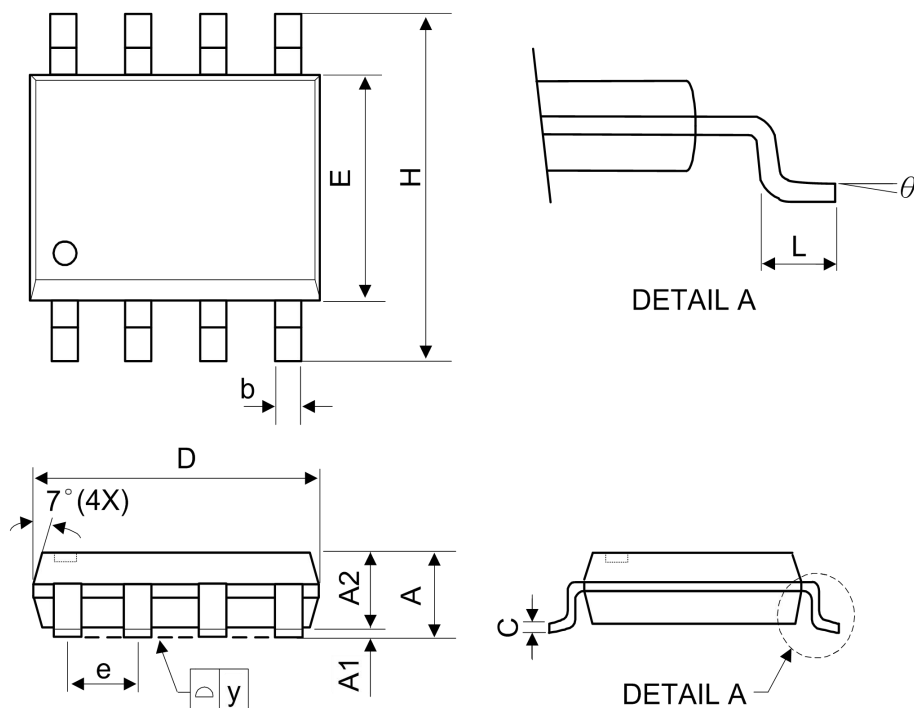
NE1289 Demo Board Layout (Bottom Layer)



NE1289 Demo Board Schematic

Package Information

SOP-8



Symbol	Millimetre			Inch		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.75	-	-	0.069
A1	0.1	-	0.25	0.04	-	0.1
A2	1.25	-	-	0.049	-	-
C	0.1	0.2	0.25	0.0075	0.008	0.01
D	4.7	4.9	5.1	0.185	0.193	0.2
E	3.7	3.9	4.1	0.146	0.154	0.161
H	5.8	6	6.2	0.228	0.236	0.244
L	0.4	-	1.27	0.015	-	0.05
b	0.31	0.41	0.51	0.012	0.016	0.02
e	1.27 BSC			0.050 BSC		
y	-	-	0.1	-	-	0.004
θ	0°	-	8°	0°	-	8°